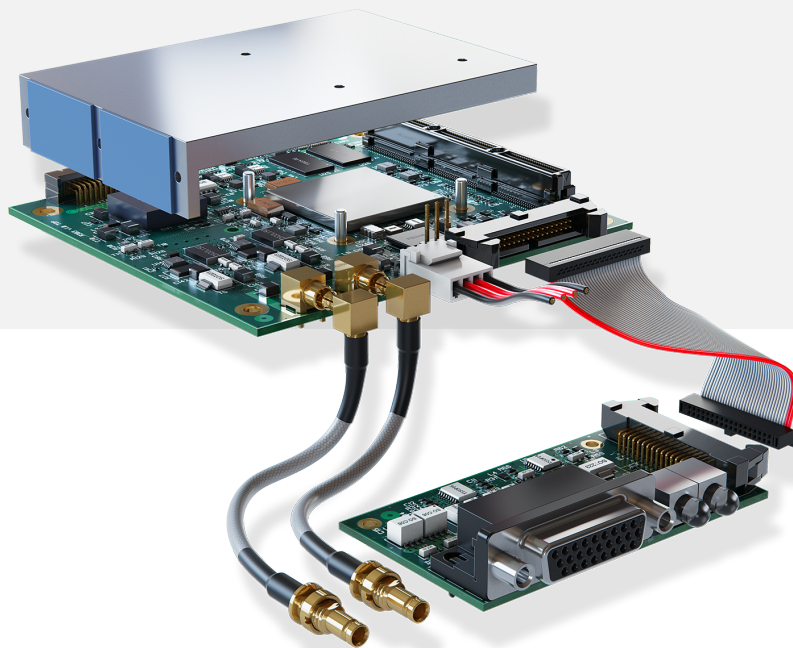


# Coaxlink

1629 Coaxlink Duo PCIe/104-EMB

1634 Coaxlink Duo PCIe/104-MIL



**CoaxPress**

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# 1. About This Document

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## 1.1. Document Scope

This document describes the **hardware specifications** of all the PCI Express/104 products of the Coaxlink series together with their related products.

### Coaxlink Products

Product	S/N Prefix	Icon
1629 Coaxlink Duo PCIe/104-EMB	KDI	<a href="#">Duo104EMB</a>
1633-LH Coaxlink Quad G3 LH	KQH	<a href="#">QuadG3LH</a>
1634 Coaxlink Duo PCIe/104-MIL	KDR	<a href="#">Duo104MIL</a>

### Related Accessories

Product	S/N Prefix	Icon
3300 HD26F I/O module for Coaxlink Duo PCIe/104		<a href="#">3300</a>
3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104		<a href="#">3301</a>
3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104		<a href="#">3302</a>

**Note:** The S/N prefix is a 3-letter string at the beginning of the card serial number.

**Note:** Icons are used in this document for tagging titles of card-specific content.

## 1.2. Document Structure

This document is composed of 4 main sections:

- ["Mechanical Specification" on the facing page](#) provides the product pictures, the physical dimensions, the connectors description and the pin assignments, the lamps description, etc.
- ["Electrical Specification" on page 27](#) provides the electrical characteristics of all input/output ports, a description of the power distribution, power requirements, etc.
- ["Environmental Specification" on page 45](#) provides the climatic requirements and CE/FCC/RoHS/WEEE compliance statements.
- ["Related Products & Accessories" on page 52](#) provides a description of related products and accessories such as adapters, cables ...

## 1.3. Document Revision History

Date	Document Version	Description
2016-07-29	1.0	First edition.
2017-02-13	2.0	Second edition <ul style="list-style-type: none"> <li>• Add 1629 Coaxlink Duo PCIe/104-EMB</li> <li>• Add 1634 Coaxlink Duo PCIe/104-MIL</li> </ul>
2017-10-27	2.1.0	Specification updates: <ul style="list-style-type: none"> <li>• <a href="#">"TTL Input/Output" on page 39</a>: revised DC and AC electrical specifications of TTL I/O ports</li> </ul>

## 2. Mechanical Specification

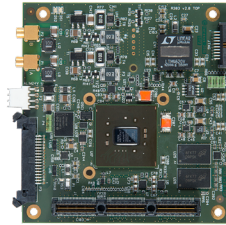
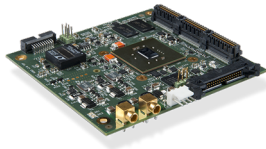
*Mechanical specifications of the product(s) including: product pictures, physical dimensions, connectors description and pin assignments, lamps description, switches description, etc.*

2.1. Product Pictures .....	8
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## 2.1. Product Pictures

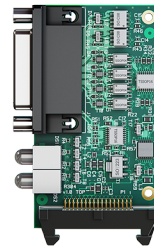
### 1629 Coaxlink Duo PCIe/104-EMB

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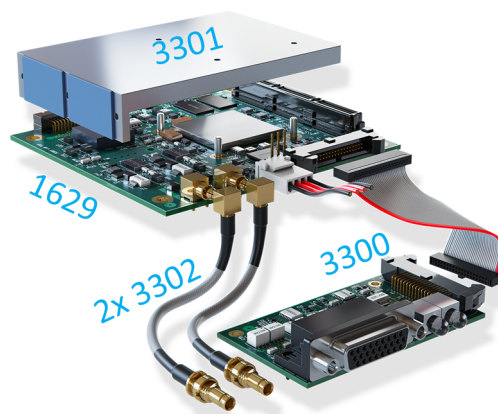
### 3300 HD26F I/O module for Coaxlink Duo PCIe/104

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### 1629 Coaxlink Duo PCIe/104-EMB System Assembly

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1629 Coaxlink Duo PCIe/104-EMB with 3300 HD26F I/O module for Coaxlink Duo PCIe/104 , 3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104 and 2 3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104



## 2.2. Physical Characteristics

### Dimensions and Weight - PCIe/104 Products

Product Item	Length	Width	Weight
1629 Coaxlink Duo PCIe/104-EMB	96 mm, 3.775 in	90 mm, 3.555 in	75 g, 2.65 oz
1634 Coaxlink Duo PCIe/104-MIL	96 mm, 3.775 in	90 mm, 3.555 in	75 g, 2.65 oz
3300 HD26F I/O module for Coaxlink Duo PCIe/104 – Module	70 mm, 2.76 in	40 mm, 1.57 in	60 g, 2.12 oz
3300 HD26F I/O module for Coaxlink Duo PCIe/104 – Cable	254 mm, 10 in		
3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104	86.8 mm, 3.42 in	60 mm, 2.36 in	75 g, 2.65 oz
3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104	200 mm, 7.9 in		

### 3D CAD Models - PCIe/104 Products

3D CAD models are available on request for the following assemblies:

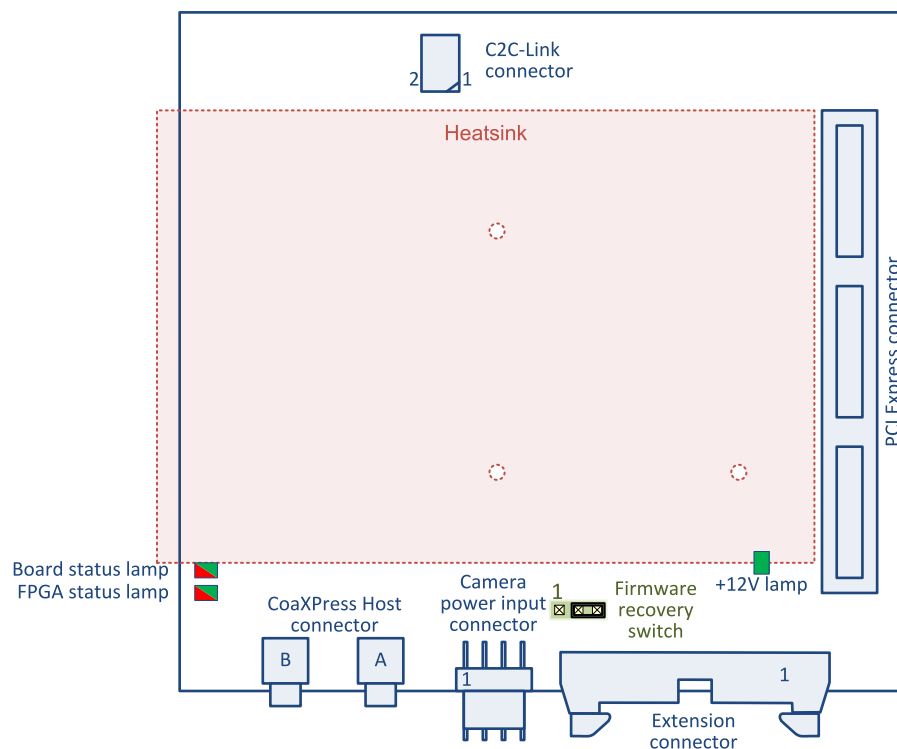
Assembly	File formats
1629 Coaxlink Duo PCIe/104-EMB	DWF, STP
1629 Coaxlink Duo PCIe/104-EMB with 3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104	DWF, STP
3300 HD26F I/O module for Coaxlink Duo PCIe/104	DWF, STP

## 2.3. Connectors, Lamps and Switches

# Bracket and Board Layouts

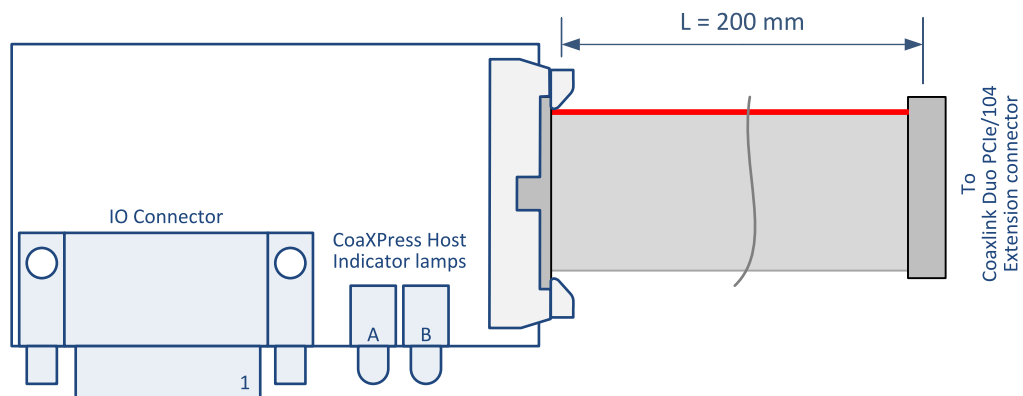
*Layouts of connectors, lamps, switches and main components*

## 1629 Coaxlink Duo PCIe/104-EMB and 1634 Coaxlink Duo PCIe/104-MIL



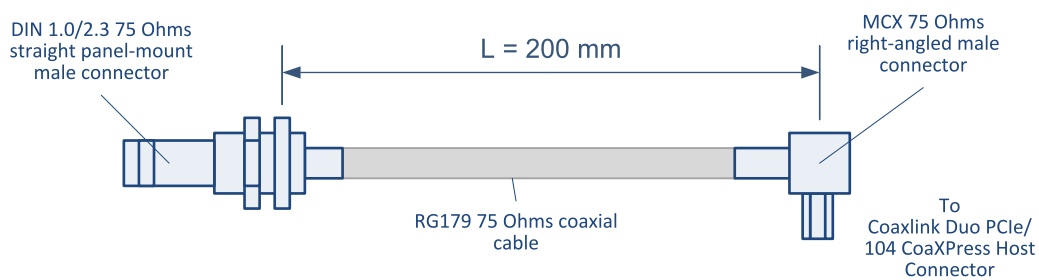
- "CoaXPress Host A Connector" on page 14
- "CoaXPress Host B Connector" on page 15
- "C2C-Link Connector" on page 18
- "12V Lamp " on page 21
- "Board Status Lamp" on page 22
- "FPGA Status Lamp" on page 23
- "Firmware Recovery Switch" on page 24

### 3300 HD26F I/O module for Coaxlink Duo PCIe/104



- "I/O Connector" on page 16
- "CoaXPress Lamps" on page 20

### 3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104



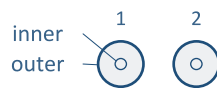
- "DIN-2 CoaXPress Host Connector" on the next page

# DIN-2 CoaXPress Host Connector

Applies to: **Duo104EMB**

## Connector description

Property	Value
Name	DIN-2 CoaXPress Host
Type	2 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Module-to-chassis coaxial cables
Usage	CoaXPress Host Interface CoaXPress Data Forwarding Interface



## Pin assignments

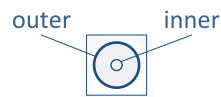
Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground

# CoaXPress Host A Connector

Applies to: [Duo104EMB](#) [Duo104MIL](#)

## Connector description

Property	Value
Name	CoaXPress Host A
Type	MCX 75 Ohms coaxial female receptacle
Location	Printed circuit board
Usage	CoaXPress Host Interface CoaXPress Data Forwarding Interface



## Pin assignments

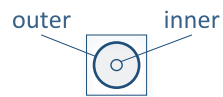
Pin	Signal	Usage
Inner	CXP_A	CoaXPress Host Connection A
Outer	GND	Ground

# CoaXPress Host B Connector

Applies to: [Duo104EMB](#) [Duo104MIL](#)

## Connector description

Property	Value
Name	CoaXPress Host B
Type	MCX 75 Ohms coaxial female receptacle
Location	Printed circuit board
Usage	CoaXPress Host Interface CoaXPress Data Forwarding Interface



## Pin assignments

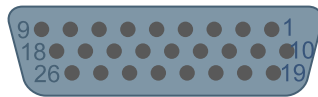
Pin	Signal	Usage
Inner	CXP_B	CoaXPress Host Connection B
Outer	GND	Ground

# I/O Connector

Applies to: **Duo104EMB**

## Connector description

Property	Value
Name	I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Remote I/O module
Usage	General purpose I/O and power output



## Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN12+	High-speed differential input #12 – Positive pole
3	IIN11+	Isolated input #11 – Positive pole
4	IIN13-	Isolated input #13 – Negative pole
5	IIN14-	Isolated input #14 – Negative pole
6	IOOUT12-	Isolated contact output #12 – Negative pole
7	GND	Ground
8		Not connected
9	GND	Ground
10	GND	Ground
11	DIN12-	High-speed differential input #12 – Negative pole
12	IIN11-	Isolated input #11 – Negative pole
13	IIN12+	Isolated input #12 – Positive pole
14	IIN13+	Isolated input #13 – Positive pole
15	IIN14+	Isolated input #14 – Positive pole



Pin	Signal	Usage
16	IOUT12+	Isolated contact output #12 – Positive pole
17	TTLIO12	TTL input/output #12
18	GND	Ground
19	DIN11-	High-speed differential input #11 – Negative pole
20	DIN11+	High-speed differential input #11 – Positive pole
21	IIN12-	Isolated input #12 – Negative pole
22	IOUT11-	Isolated contact output #11 – Negative pole
23	IOUT11+	Isolated contact output #11 – Positive pole
24	GND	Ground
25	TTLIO11	TTL input/output #11
26	+12V	+12 V Power output

# C2C-Link Connector

Applies to: [Duo104EMB](#) [Duo104MIL](#)

## Connector description

Property	Value
Name	C2C-Link
Type	6-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	Card-to-card link



## Pin assignments

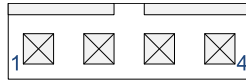
Pin	Signal	Usage
1	GND	Ground
2	CSync1	Card-to-card synchronization bus – Signal 1
3	GND	Ground
4	CSync2	Card-to-card synchronization bus – Signal 2
5	GND	Ground
6	CSync3	Card-to-card synchronization bus – Signal 3

# Camera Power Input Connector

Applies to: [Duo104EMB](#) [Duo104MIL](#)

## Connector description

Property	Value
Name	Camera Power Input
Type	4-pin 0.1-in Molex KK 7478 male connector
Location	Printed circuit board
Usage	DC power input for PoCXP











## Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	+24V0	+24 VDC input
3	+24V0	+24 VDC input
4	GND	Ground

## CoaXPress Lamps

Each connector of the CoaXPress Host Interface is associated with a *CoaXPress Host Indicator Lamp* that indicates the state of the CoaXPress Link connection.

### CoaXPress Host Connector Indicator Lamps State

Symbol	Lamp State	Meaning
	Off	The Coaxlink card is not powered
	Solid orange	System booting
	Fast flash alternate green / orange	The connection detection is in progress; PoCXP is active. <i>This state is shown for a minimum of 1s even if the connection detection is faster</i>
	Fast flash orange	The connection detection is in progress; PoCXP is off. <i>This state is shown for a minimum of 1s even if the connection detection is faster</i>
	Solid red	The PoCXP over-current protection has tripped.
	Solid green	The Device to Host connection is established, but no data being transferred
	Slow pulse orange	The Device to Host connection is established, but the Host is waiting for a trigger.
	Fast flash green.	The Device to Host connection is established and image data is being transferred

### Flashing Lamp States Timing Definitions

Indication	Timing
Fast flash	<b>12.5Hz @25% duty cycle:</b> 20 ms on, 60 ms off
Fast flash alternate (color 1/color 2)	<b>12.5Hz @25% duty cycle:</b> 20 ms on (color 1), 60 ms off, 20 ms on (color 2), 60 ms off
Slow flash	<b>0.5Hz @50% duty cycle:</b> 1 second on, 1 second off
Slow pulse (red   orange)	<b>1Hz @ 20% duty cycle:</b> 200ms on, 800ms off



# 12V Lamp

Duo104EMB

Duo104MIL




## 12V lamp states

---

Lamp state	Symbol	Meaning
Off		<b>No +12V power.</b> Possible causes are: <ul style="list-style-type: none"><li>• There is no power delivered on the +12 V rail of the PCIe/104 connector</li><li>• The +12V fuse is blown on the card</li></ul>
Solid green		<b>12V power OK.</b>

# Board Status Lamp




## Board status lamp indicator states

Lamp state	Symbol	Meaning
Off		<p><b>No power.</b></p> <p>The board is not powered or the power distribution network is not functional.</p>
Solid green		<p><b>Board status OK.</b></p> <p>The main power distribution network is operational and the FPGA start-up procedure has successfully completed.</p>
Solid red		<p><b>Board status NOK.</b></p> <p>Possible causes are:</p> <ul style="list-style-type: none"> <li>• There is no power delivered on the +12 V rail of the PCI Express connector slot</li> <li>• The FPGA start-up procedure is not completed. <i>The normal completion time is around 100 milliseconds.</i></li> <li>• At least one power converter of the main power distribution network is unable to operate properly. <i>This might be caused by excessive temperature due to inadequate board cooling, accidental short-circuits having blown one (or more) protection fuses, inappropriate supply voltages, etc.</i></li> </ul>

# FPGA Status Lamp

## FPGA status lamp indicator states

---

Lamp state	Symbol	Meaning
Off		<b>Board not powered.</b>
Solid green		<b>FPGA status OK.</b> All the FPGA clock networks and the DDR memory are operating normally.
Solid red		<b>FPGA status NOK.</b> Possible causes are: <ul style="list-style-type: none"><li>• At least one FPGA clock network is not operating normally. <i>This might be caused by excessive jitter on external clock signals of the CoaXPress or the PCI Express interfaces.</i></li><li>• The DDR memory controller has not been able to successfully perform the calibration procedure.</li></ul>

# Firmware Recovery Switch

The firmware recovery switch is implemented with a 3-pin 1-row header and a jumper. The jumper has two positions: **normal** and **recovery**.

## Normal position

At the next power ON, the latest firmware successfully written into the Flash EEPROM is used to program the FPGA.

After FPGA startup completion, the card exhibits the standard PCI ID and the Coaxlink driver allows normal operation.

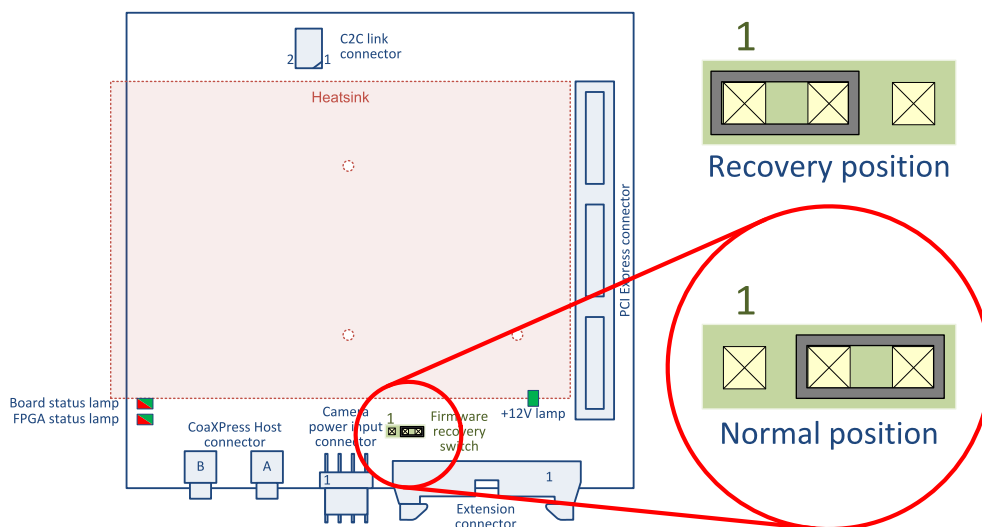
This is the factory default jumper position.

## Recovery position

At the next power ON, the last but one firmware successfully written into the Flash EEPROM is used to program the FPGA.

After FPGA startup completion, the card exhibits the recovery PCI ID and the Coaxlink driver inhibits image acquisition.

## 1629 Coaxlink Duo PCIe/104-EMB, 1634 Coaxlink Duo PCIe/104-MIL





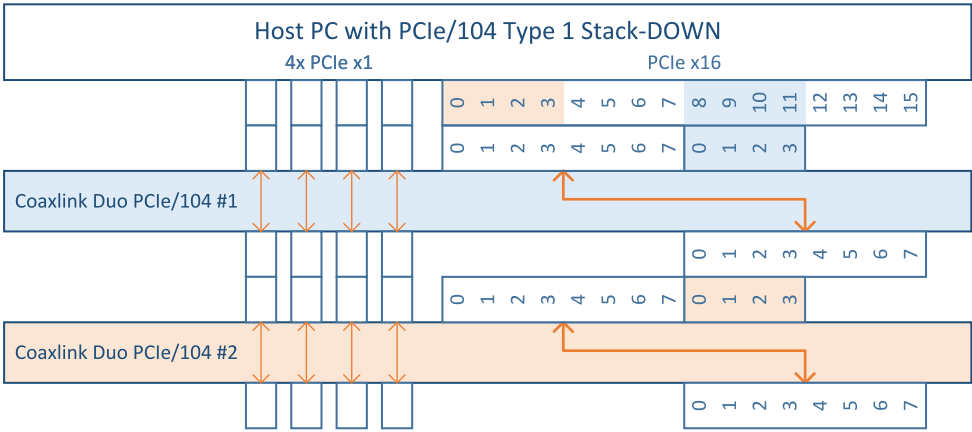
# 2.4. PCIe/104 Stacking Rules

One or two 1629 Coaxlink Duo PCIe/104-EMB or 1634 Coaxlink Duo PCIe/104-MIL modules can be stacked directly under the Host PC.

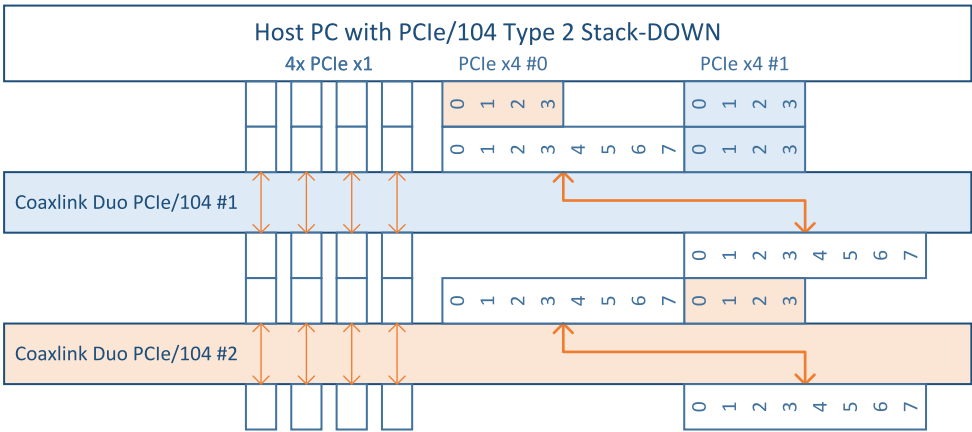
The Host PC must be equipped with one **stack-down** connector of the following types:

- Type 2 PCIe/104 with 2 PCI Express x4 links providing four active lanes.
- Type 1 PCIe/104 with 1 PCI Express x16 link configured to operate as 2 x8 links providing at least four active lanes per link.

**Note:** According the PCIe/104 specification, a Type 1 PCIe/104 host PC that supports a PCIe x16 link is not required to support two x8, or two x4 links. For such PCs, only one module can be stacked underneath!



**PCIe/104 stack with a Type 1 Host PC and 2 modules.**



**PCIe/104 stack with a Type 2 Host PC and 2 modules.**

Each module:

- Uses only 4 PCI Express lanes.
- Routes to the next module the 4 unused PCI Express x1 links.
- Shifts by 8 positions and routes to the next module the lowest 8 lanes of the PCI Express x16 link.
- Re-drives the clock of the Type 1 PCI Express x16 or the Type 2 PCI Express x4 links.

# 3. Electrical Specification

*Electrical specification of the product(s) including: electrical characteristics of all the input/output ports, description of the power distribution, power requirements, etc.*

3.1. CoaXPress Host Interface .....	28
3.2. PCI Express Interface .....	30
3.3. Power Distribution .....	31
3.4. PCI Express Power .....	34
3.5. Camera Power Input .....	35
3.6. I/O Power Output .....	36
3.7. Differential Input .....	37
3.8. TTL Input/Output .....	39
3.9. Isolated Input .....	41
3.10. Isolated Output .....	43

## 3.1. CoaXPress Host Interface

*Electrical specification of the CoaXPress Host interface*

### CoaXPress Host Interface Type per Product

Each connection of the CoaXPress Host interface implements a **Host Transceiver** (HT) and a **Power Transmitting Unit** (PTU).

Product	HT Type
1629 Coaxlink Duo PCIe/104-EMB	"CXP-6 Host Transceiver" below
1634 Coaxlink Duo PCIe/104-MIL	"CXP-6 Host Transceiver" below

### CXP-6 Host Transceiver

Applies to: [QuadG3LH](#) [Duo104EMB](#) [Duo104MIL](#)

The Host transceiver implements a **high-speed cable receiver** and a **low-speed cable driver** for **CXP-6** speeds.

It fulfills the electrical specification of the CoaXPress 1.1 standard. Namely:

- The cable receiver requirements for the high-speed connection described in Table 2 of the Annex B of the CoaXPress Standard 1.1
- The cable driver requirements for the low-speed connection described in Table 3 of the Annex B of the CoaXPress Standard 1.1

#### Host Transceiver Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
High-speed connection bit rate		1.25		6.25	GT/s
Low-speed connection bit rate			20.833		MT/s
Max. cable length	BELDEN 1694 @ 1.25 GT/s	130			m
	BELDEN 1694 @ 2.5 GT/s	110			m
	BELDEN 1694 @ 3.125 GT/s	100			m
	BELDEN 1694 @ 5 GT/s	60			m
	BELDEN 1694 @ 6.25 GT/s	40			m

### Power Transmitting Unit

The Power Transmitting Unit implements Power over CoaXPress (PoCXP) as specified in section 7 of the CoaXPress Standard 1.1.

If fulfills all the requirements for a Host; namely:

- Over-current protection (OCP)
- PoCXP CoaXPress Device detection

In addition: it provides the user with an AUTO/OFF control:

- Setting the control to AUTO initiates a new PoCXP device detection; the power will be applied only if the detection succeeds
- Setting the control to OFF forces the PTU to disconnect. *The control is OFF after power on, and, if providing power to the camera is required, has to be set to AUTO by the application.*

### Power Transmitting Unit Specification

Parameter	Min.	Typ.	Max.	Unit
DC output voltage	22	24	26	V
Available output power	17			W
OCP holding current	790			mA
OCP nominal trip current			5	A
PoCXP Device detection sensing current	550		1,000	μA

**Note:** *The above specification applies over the whole operating temperature range of the Coaxlink card.*

## 3.2. PCI Express Interface

### Specification of the PCI Express Interface

The PCI Express Interface implements a **PCIe end-point** interface and provides **electrical power** to the Coaxlink card.

### PCI Express End-point Type per Product

Product	Type
1629 Coaxlink Duo PCIe/104-EMB	"4-lane Rev 2.0 PCIe End-point" below
1634 Coaxlink Duo PCIe/104-MIL	"4-lane Rev 2.0 PCIe End-point" below

### 4-lane Rev 2.0 PCIe End-point

Applies to: [Duo104EMB](#) [Duo104MIL](#)

The 4-lane Rev 2.0 PCIe end-point:

- complies with Revision 2.0 of the PCI Express Card Electromechanical specification.
- supports 1-lane, 2-lane, and 4-lane link width
- supports PCIe Rev 2.0 link speed (5.0 GT/s with 8b/10b coding)
- supports PCIe Rev 1.0 link speed (2.5 GT/s with 8b/10b coding)
- supports payload size up to 512 bytes
- offers the optimal performance when it is configured for 4-lane PCIe Rev 2.0 link speed (5 GT/s)

### 4-lane Rev 3.0 PCIe end-point to PC memory data transfer performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	4-lane @ 5 GT/s (PCIe Rev 2.0)		1,600		MB/s
	4-lane @ 2.5 GT/s (PCIe Rev 1.0)		800		MB/s
	2-lane @ 5 GT/s (PCIe Rev 2.0)		800		MB/s

## 3.3. Power Distribution

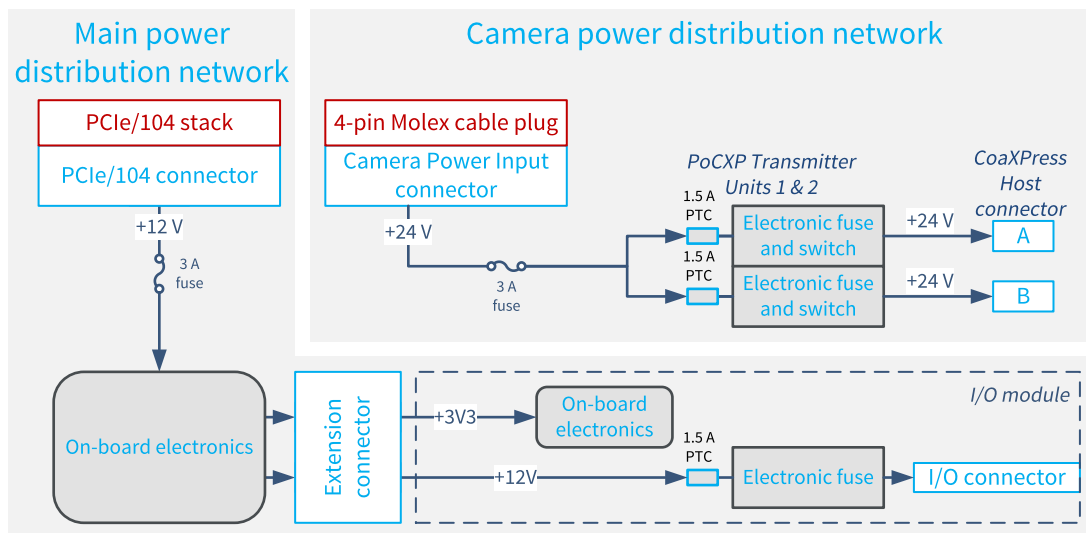
*Description of the power distribution*

### Power Distribution Schemes of PCIe/104 Products

#### 1629 Coaxlink Duo PCIe/104-EMB Power Distribution Scheme

The power distribution scheme has two distinct distribution networks:

- The main power distribution network
- The camera power distribution network



**Note:** The fuses are not serviceable! When blown, the card must be returned to the factory.

**Note:** PTCs and electronic fuses are self-resettable fuses.

**Note:** The Coaxlink card can be operated without applying power to the camera power distribution network.

The **main power distribution network** delivers power to **all the on-board electronic devices** including FPGA, memory chips, CoaXPress transceivers, I/O drivers and receivers, fan motor.

It also delivers +3.3V and +12V to the 3300 HD26F I/O module for Coaxlink Duo PCIe/104 plugged on the extension connector:

- The +3.3V is used for powering the on-board electronics: I/O drivers, I/O receivers
- The +12V is used for delivering power on the I/O connector. A PTC inserted at the input prevents potential fire hazards.

The network is fed by the Host PC through the +12 V power rail of the PCIe/104 connector. A protection fuse prevents potential fire hazards. The **+12V lamp** indicates the presence of +12V after the protection fuse.

The **board status LED lamp** reflects the global status of all the power converters of the main distribution network.

The **auxiliary power distribution network** delivers power to the CoaXPress cameras using the PoCXP capability available on all connections of the CoaXPress Host connector.

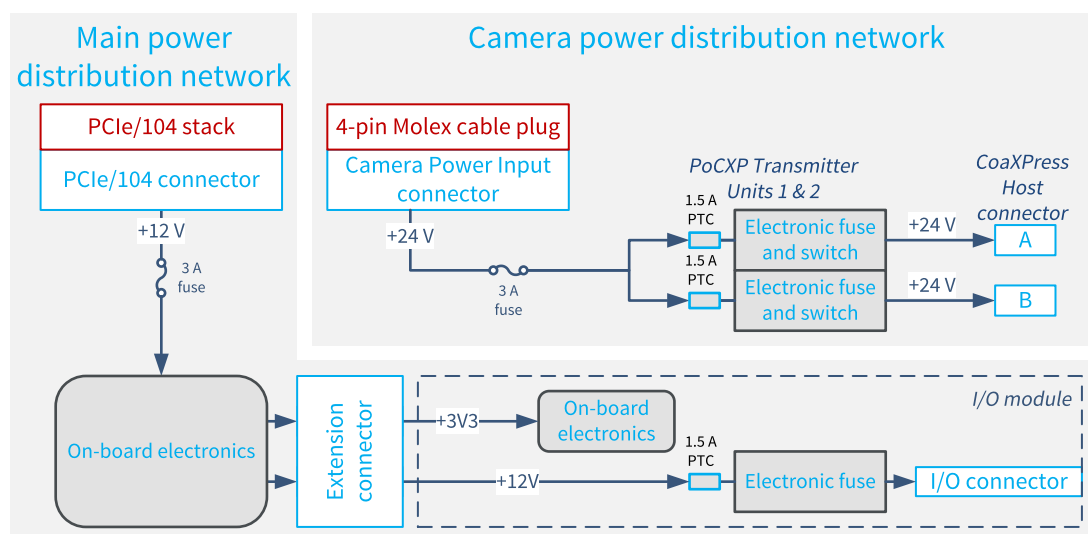
The network is fed by a 24 VDC external power supply attached to the **camera power input connector** using a power cable terminated by a 4-pin Molex plug connector. A protection fuse inserted at the input side prevents potential fire hazards.

The 24-volt DC power is applied to each camera connection through a PoCXP transmitter unit. Each PoCXP transmitter unit implements an electronic fuse/switch. A PTC inserted at the input of each transmitter unit prevents potential fire hazards.

### 1634 Coaxlink Duo PCIe/104-MIL Power Distribution Scheme

The power distribution scheme has two distinct distribution networks:

- The main power distribution network
- The camera power distribution network



**Note:** The fuses are not serviceable! When blown, the card must be returned to the factory.

**Note:** PTCs and electronic fuses are self-resettable fuses.

**Note:** The Coaxlink card can be operated without applying power to the camera power distribution network.

The **main power distribution network** delivers power to **all the on-board electronic devices** including FPGA, memory chips, CoaXPress transceivers, I/O drivers and receivers, fan motor.



It also delivers +3.3V and +12V to the **\*\*\*TBD\*\*\*** I/O module plugged on the extension connector:

- The +3.3V is used for powering the on-board electronics: I/O drivers, I/O receivers
- The +12V is used for delivering power on the I/O connector. A PTC inserted at the input prevents potential fire hazards.

The network is fed by the Host PC through the +12 V power rail of the PCIe/104 connector. A protection fuse prevents potential fire hazards. The **+12V lamp** indicates the presence of +12V after the protection fuse.

The **board status LED lamp** reflects the global status of all the power converters of the main distribution network.

The **auxiliary power distribution network** delivers power to the CoaXPress cameras using the PoCXP capability available on all connections of the CoaXPress Host connector.

The network is fed by a 24 VDC external power supply attached to the **camera power input connector** using a power cable terminated by a 4-pin Molex plug connector. A protection fuse inserted at the input side prevents potential fire hazards.

The 24-volt DC power is applied to each camera connection through a PoCXP transmitter unit. Each PoCXP transmitter unit implements an electronic fuse/switch. A PTC inserted at the input of each transmitter unit prevents potential fire hazards.

## 3.4. PCI Express Power

*PCI Express power requirements specification*

### 1629 Coaxlink Duo PCIe/104-EMB

Parameter	Conditions	Min.	Typ.	Max.	Units
+12 V voltage		11.0	12.0	13.0	V
+12 V power	No I/O module		8.4		W
	With I/O module, excluding I/O power output		TBD		W

### 1634 Coaxlink Duo PCIe/104-MIL

Parameter	Conditions	Min.	Typ.	Max.	Units
+12 V voltage		11.0	12.0	13.0	V
+12 V power	No I/O module		TBD		W
	With I/O module, excluding I/O power output		TBD		W

The typical power values were measured under the following conditions:

- Acquiring image data using all CoaXPress Host Interface connections operating at their maximum speed
- Delivering image data on the PCI Express configured for the largest link width and the highest link speed
- Operating @25°C [77 °F] ambient temperature and nominal supply voltages

## 3.5. Camera Power Input

Applies to: [Duo104EMB](#) [Duo104MIL](#)

### Specification of the Camera Power Input

**Note:** This requirement is inherited from the CoaXPress 1.0 Standard specification for Host devices.

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		23	24	25	V
DC input power	1-connection PoCXP			17	W
	2-connection PoCXP			34	W

## 3.6. I/O Power Output

### *Specification of the +12V power output of the I/O connector*

A non-isolated +12 V power output is available on every I/O connector.

The power originates from an external 12 V power supply plugged into the Auxiliary Power Input connector. It is distributed from a common electronic fuse to all the I/O connectors.

The electronic fuse provides the following protections:

- Limits the inrush current during power on sequence
- Protects the Coaxlink card and the power source against overload
- Protects the Coaxlink card the power source against short-circuits.

The sum of the load currents drawn from all the 12 V outputs of the I/O connectors must be lower or equal to the specified maximum output current.

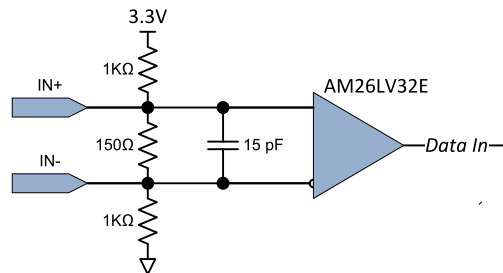
### *I/O +12 V power output specification*

Parameter	Conditions	Min.	Typ.	Max.	Units
Aggregated output current	Operating temperature range			1.0	A
Voltage drop across the electronic fuse	Max. output current			0.2	V

**Note:** *The above specification applies over the whole operating temperature range of the Coaxlink card.*

## 3.7. Differential Input

Specification of the differential GPIO input ports



**Differential Input Simplified Schematic**

The receiver complies with the ANSI/TIA/EIA-422B specification.

### DC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Common mode voltage		-7		+7	V
Differential sensitivity				200	mV
Input impedance			120		Ohm
ESD protection	Human Body Model (HBM)	15			kV
	Contact discharge	8			kV
	Air gap discharge	15			kV

### AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	100			ns
Pulse rate	0		5	MHz
10%-90% rise/fall time			1	μs

## Logical map

---

The state of the port is reported as follows:

Differential Input voltage	Logical State
$(VIN+ - VIN-) > +200 \text{ mV}$	HIGH
$(VIN+ - VIN-) < - 200 \text{ mV}$	LOW
Unconnected input	HIGH

## Compatible drivers and receivers

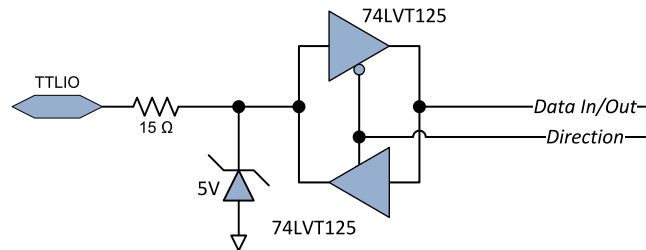
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The following drivers are compatible with the high-speed differential input ports:

- ANSI/EIA/TIA-422/485 differential line drivers
- Complementary TTL drivers

## 3.8. TTL Input/Output

Specification of the TTL GPIO input/output ports



TTL Input/Output Simplified schematic

The receiver is LVTTTL and 5 V TTL compliant. The driver is a 3.3 V TTL driver.

### DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Common mode input voltage		0		5	V
Low-level output current				64	mA
Low-level output voltage	@ 8 mA		0.34	0.36	V
	@ 16 mA		0.48	0.55	V
	@ 32 mA		0.78	0.81	V
	@ 64 mA		1.34	1.36	V
High-level output current				-32	mA
High-level output voltage	@-8 mA; (1)	2.60	3.00		V
	@-16 mA; (1)	2.20	2.70		V
	@-32 mA; (1)	1.75	2.20		V
ESD protection	Human Body Model (HBM)	2			kV

**Condition (1):** 300 Ohms line termination resistor to GND.

**Note:** The I/O port includes a latch-up protection.

## AC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Pulse width		100			ns
Pulse rate		0		5	MHz
10%-90% rise/fall time	(1)		10	20	ns

**Condition (1):** Short cable (1 m) and a 300 Ohms line termination resistor to GND.

## Logical Map

The state of the port is reported as follows:

Input voltage	Logical State
VIN > 2.0 V	HIGH
VIN < 0.8 V	LOW
Unconnected input port	<i>Undetermined</i>

## Compatible drivers and receivers

The following drivers are compatible:

- Totem-pole LVTTTL, TTL, 5 V CMOS drivers

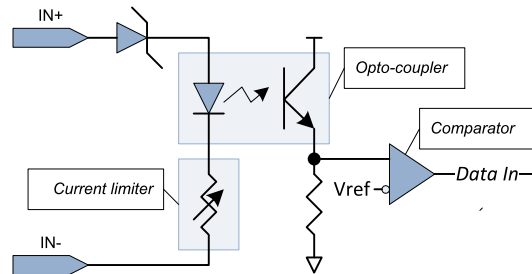
The following receivers are compatible:

- LVTTTL, TTL, 3-Volt CMOS receivers



# 3.9. Isolated Input

Specification of the isolated GPIO input ports

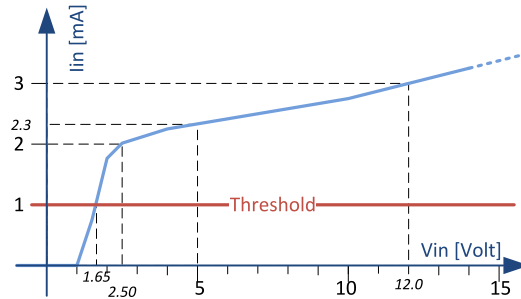


**Isolated Input Simplified schematic**

The input port implements an isolated current-sense input.

## DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential voltage		-30		+30	V
Input current threshold			1		mA
Differential voltage	@1 mA	1.5	1.65	1.9	V
Input current	@(VIN+ - VIN-) = 1.65 V		1		mA
	@(VIN+ - VIN-) = 2.5 V		2		mA
	@(VIN+ - VIN-) = 5 V		2.3		mA
	@(VIN+ - VIN-) = 12 V		3		mA
	@(VIN+ - VIN-) = 30 V			5	mA
	@(VIN+ - VIN-) < 1 V			10	µA
DC isolation voltage		250			V
AC isolation voltage		170			V <sub>RMS</sub>



**Input Current vs. Input Voltage Characteristics**

### AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	10			$\mu$ s
Pulse rate	0		50	kHz

### Logical map

The state of the port is reported as follows:

Input current	Logical State
$I_{IN} > 1 \text{ mA}$	HIGH
$I_{IN} < 1 \text{ mA}$	LOW
Unconnected input port	LOW

### Compatible drivers and receivers

The following drivers are compatible with the isolated current-sense inputs:

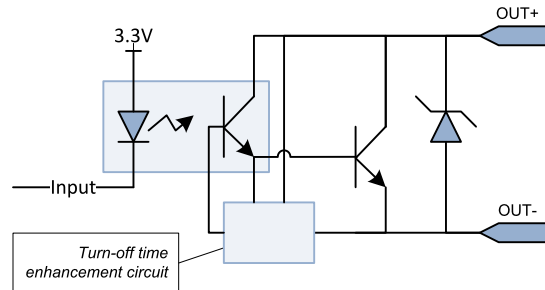
- Totem-pole LVTTTL, TTL, 5 V CMOS drivers
- RS-422 Differential line drivers
- Potential free contact, solid-state relay, or opto-isolators
- 12 V and 24 V signaling voltages are also accepted

**Note:** The +12 V power supply on the I/O connector(s) can be used for powering drivers requiring a power supply.

**Note:** No external resistors are required. However, to obtain the best noise immunity with 12 V and 24 V signaling, it is recommended to insert a series resistor in the circuit. The recommended resistor values are: 4.7k Ohms for 12 V signaling and 10k Ohms for 24 V signaling.

## 3.10. Isolated Output

Specification of the isolated GPIO output ports



Isolated Output Simplified schematic

The output port implements an isolated contact output.

### DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Current				100	mA
Differential voltage	Open state	-30		30	V
	Closed state @ 1 mA			0.4	V
	Closed state @ 100 mA			1.0	V
DC isolation voltage		250			V
AC isolation voltage		170			V <sub>RMS</sub>

**Note:** The output port in the closed state has no current limiter, the user circuit must be designed to avoid excessive currents that could destroy the output port.

**Note:** The output port remains in the OFF-state until it is under control of the application.

### AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse rate	0		100	kHz
Turn-on time			5	μs
Turn-off time			5	μs

### Typical switching performance @ 25°C

Current [mA]	Turn ON time [ $\mu$ s]	Turn OFF time [ $\mu$ s]
0.5	2.0	4.8
1.0	2.0	3.9
4.0	2.2	3.3
10	2.3	2.7
40	2.3	2.7
100	2.3	2.7

### Logical map

The state of the output port is determined as follows:

Logical State	Output port state
HIGH	The contact switch is closed (ON)
LOW	The contact switch is open (OFF)

### Compatible loads

The following loads are compatible with the isolated contact output ports:

- Any load within the 30V / 100 mA envelope is accepted. The power originates from an external power source or alternatively from the power delivered through the 12V and GND pins of the I/O connectors.

# 4. Environmental Specification

*Environmental specification of the product(s) including: climatic requirements, electromagnetic standards compliance statements, safety standards compliance statements, etc.*

- 4.1. Environmental Conditions ..... 46
- 4.2. Thermal Data ..... 48
- 4.3. Compliances ..... 49

## 4.1. Environmental Conditions

Storage and operating conditions specification of standard climatic class products

### Storage Conditions

Applies to: **Duo104EMB**

Parameter	Conditions	Min	Max	Units
Ambient air temperature		-20 [-4]	70 [158]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

Applies to: **Duo104MIL**

Parameter	Conditions	Min	Max	Units
Ambient air temperature		TBD	70 [158]	°C [°F]
Ambient air humidity	Non-condensing	TBD	TBD	% RH

### Operating Conditions

Applies to: **Duo104EMB**

Parameter	Conditions	Min	Max	Units
FPGA die temperature			80 [176]	°C [°F]
Ambient air temperature		0 [32]	50 [122]	°C [°F]
Ambient air humidity	Non-condensing	0	100	% RH

Applies to: **Duo104MIL**

Parameter	Conditions	Min	Max	Units
FPGA die temperature			100 [212]	°C [°F]
Ambient air temperature	Conduction-cooling	-40 [-40]	85 [185]	°C [°F]
Ambient air humidity	Non-condensing	0	100	% RH
Shock amplitude	All axes – 11 ms duration – Half-sine and saw tooth pulse shapes		20	g

**Important:** The thermal design of the host PC must ensure that, at any time, the FPGA die temperature never exceeds the recommended limit.

**Warning:** Exceeding the upper limit of the FPGA die temperature can permanently damage the card.

**Note:** *The Coaxlink cards are equipped with a temperature sensor that reports the temperature of the FPGA die.*

**Note:** *An event is reported to the application when the FPGA die temperature reaches the limit.*

**Note:** *For PCIe/104 products only, the ambient air temperature specification applies to any point in the vicinity of the module including the gap between modules of the PCIe/104 stack.*

## 4.2. Thermal Data

*Heat sources and heat extraction method*

### PCIe/104 Products

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Applies to: [Duo104EMB](#) [Duo104MIL](#)

The main heat contributors are the electronic devices of the main card. This includes the losses of the power converters of the main power distribution network.

#### *Estimated heat power [W]*

Product	Main	Auxiliary	Total
1629 Coaxlink Duo PCIe/104-EMB	8.4	-	8.4
1634 Coaxlink Duo PCIe/104-MIL	8.4	-	8.4

The heat produced by the board is conducted to the chassis enclosure using a heatsink such as the 3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104

The thermal design of the PCIe/104 system must ensure an adequate cooling of the enclosure to keep the FPGA die temperature and the ambient air temperature below the upper limits of the allowed temperature range. The application is responsible for regularly checking the temperature and for taking the appropriate action in case of excessive temperature.



## 4.3. Compliances

*Compliance statements.*

### CE Compliance Statement

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Applies to: **QuadG3LH** **Duo104EMB**



#### Notice for Europe

This product is in conformity with the Council Directive 2014/30/EU

This piece of equipment has been tested and found to comply with Class B EN55022/CISPR22 electromagnetic emission requirements and Class A EN55024/CISPR24 electromagnetic susceptibility.

This product has been tested in typical class A and class B compliant host systems. It is assumed that this product will also achieve compliance in any class A or class B compliant unit.

To meet EC requirements, shielded cables must be used to connect a peripheral to the card.

### CE Compliance Statement

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Applies to: **Duo104MIL**



#### Notice for Europe

This product is in conformity with the Council Directive 2014/30/EU

This piece of equipment has been tested and found to comply with Class B EN55022/CISPR22 electromagnetic emission requirements and Class A EN55024/CISPR24 electromagnetic susceptibility.

This product has been tested in typical class A and class B compliant host systems. It is assumed that this product will also achieve compliance in any class A or class B compliant unit.

To meet EC requirements, shielded cables must be used to connect a peripheral to the card.

### FCC Compliance Statement

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Applies to: **QuadG3LH** **Duo104EMB****Notice for USA**

Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation or when the equipment is operated in a commercial environment.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

## FCC Compliance Statement

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Applies to: **Duo104MIL****Notice for USA**

Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15

This equipment has been tested and found to comply with the limits for Class A and Class B digital devices, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation or when the equipment is operated in a commercial environment.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

## Shock and Vibrations

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Applies to: **Duo104MIL**

Half-sine and terminal peak shocks according to MIL-STD-810G method 516.6:

- 40 g/11 ms

## RoHS Compliance Statement

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This product is in conformity with the European Union RoHS 2011/65/EU Directive, that stands for "the restriction of the use of certain hazardous substances in electrical and electronic equipment".

## WEEE Statement

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According the European directive 2012/19/EU, the product must be disposed of separately from normal household waste. It must be recycled according to the local regulations.

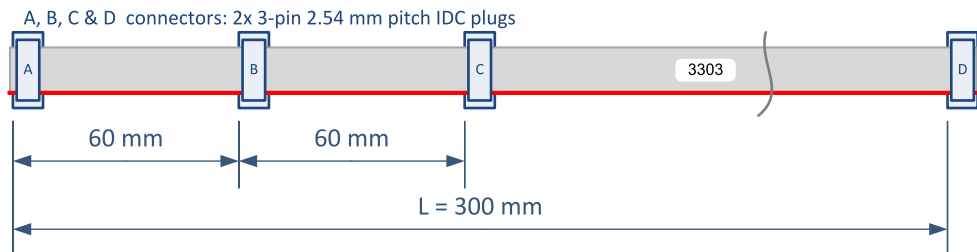
# 5. Related Products & Accessories

5.1. 3303 C2C-Link Ribbon Cable .....53  
5.2. Custom C2C-Link Ribbon Cable Assembly .....54

## 5.1. 3303 C2C-Link Ribbon Cable

3303 C2C-Link Ribbon Cable is an accessory product used for Intra-PC C2C-Link interconnection.

### 3303 C2C-Link Ribbon Cable



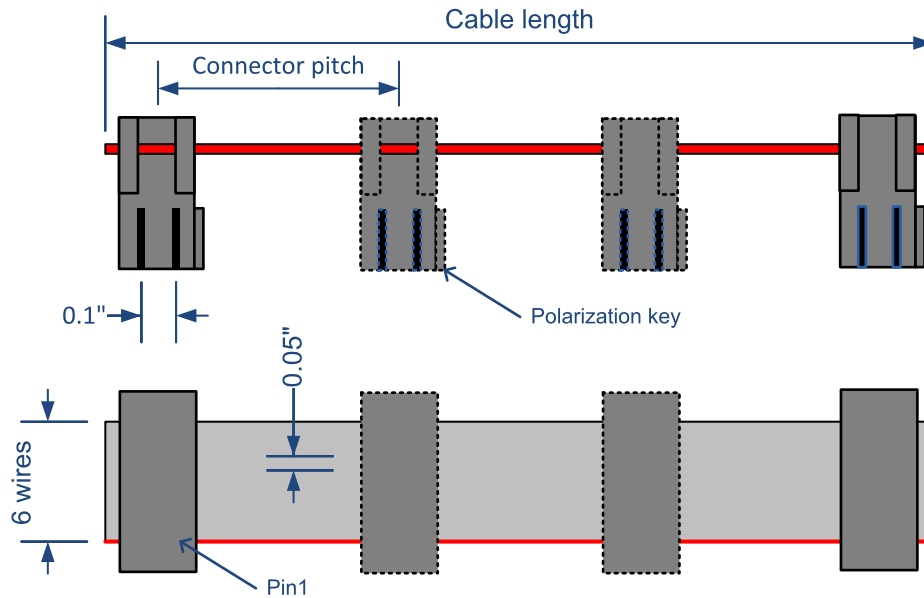
### 3303 C2C-Link Ribbon Cable assembly

The 3303 C2C-Link Ribbon Cable is a 6-conductor 0.05-in pitch ribbon fitted with 4 6-pin female ribbon cable connectors.

This cable is used for interconnecting the C2C-Link connectors of up to 4 cards located in the same PC.

## 5.2. Custom C2C-Link Ribbon Cable Assembly

Assembly instructions of a custom-made IntraPC C2C-Link interconnection.



**Custom C2C-Link Ribbon Cable Assembly**

The cable assembly is composed with:

- A piece of a 6-conductor 0.05-in pitch ribbon cable. For instance: *Belden's (9L280XX Series)*.
- Two or more pieces of a 2 x 3-pin female ribbon cable connectors. For instance: *TE connectivity 1-1658528-1*.

The cable assembly has:

- A maximum of 4 connectors allowing up to 4 cards to share the same C2C-Link.
- A maximum length of 60 cm.

**Note:** *The connector pitch(es) must be determined according to the actual card to card spacing in the Host PC.*