EURESYS™
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HARDWARE MANUAL

Coaxlink

1630 Coaxlink Mono
1631 Coaxlink Duo
1632 Coaxlink Quad
1633 Coaxlink Quad G3
1635 Coaxlink Quad G3 DF
1637 Coaxlink Quad 3D-LLE
1638 Coaxlink Quad CXP-3
3602 Coaxlink Octo
3603 Coaxlink Quad CXP-12

PCI EXPRESS™

CoaXPress

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This documentation is provided with Coaxlink 10.3.1 (doc build 2052).

Contents

1. About This Document

1.1. Document Scope

This document describes the **hardware specifications** of all the PCI Express products of the Coaxlink series together with their related products.

Coaxlink Products

Product	S/N Prefix	Icon
1630 Coaxlink Mono	KMO	Mono
1631 Coaxlink Duo	KDU	Duo
1632 Coaxlink Quad	KQU	Quad
1633 Coaxlink Quad G3	KQG	QuadG3
1635 Coaxlink Quad G3 DF	KDF	QuadG3DF
1637 Coaxlink Quad 3D-LLE	KQE	Quad3DLLE
1638 Coaxlink Quad CXP-3	KQL	QuadCXP3
3602 Coaxlink Octo	KOC	Octo
3603 Coaxlink Quad CXP-12	KQP	QuadCXP12

Related Accessories

Product	S/N Prefix	Icon
1625 DB25F I/O Adapter Cable		1625
1636 InterPC C2C-Link Adapter	KCC	1636
3303 C2C-Link Ribbon Cable		3303
3304 HD26F I/O Adapter Cable		3304

Product	S/N Prefix	Icon
3610 HD26F I/O Extension Module TTL-RS422	EMA	3610
3612 HD26F I/O Extension Module TTL-CMOS5V-RS422	EMC	3612
3613 JTAG Adapter Xilinx for Coaxlink	AXC	3613

Note: *The S/N prefix is a 3-letter string at the beginning of the card serial number.*

Note: *Icons are used in this document for tagging titles of card-specific content.*

1.2. Document Revision History

Date	Version	Description
2017-02-17	7.0	Add 1629 Coaxlink Duo PCIe/104-EMB and 1634 Coaxlink Duo PCIe/104-MIL
2017-05-24	8.0	Add 1638 Coaxlink Quad CXP-3
2017-06-08	9.0	Add 1637 Coaxlink Quad 3D-LLE
2017-10-27	9.1	Specification updates: • "TTL Input/Output" on page 68: revised DC and AC electrical specifications of TTL I/O ports • "Environmental Conditions" on page 75: extend the operating temperature range to + 55 °C
2018-05-18	10.0	Add 3602 Coaxlink Octo

1.3. Document Structure

This document is composed of 4 main sections:

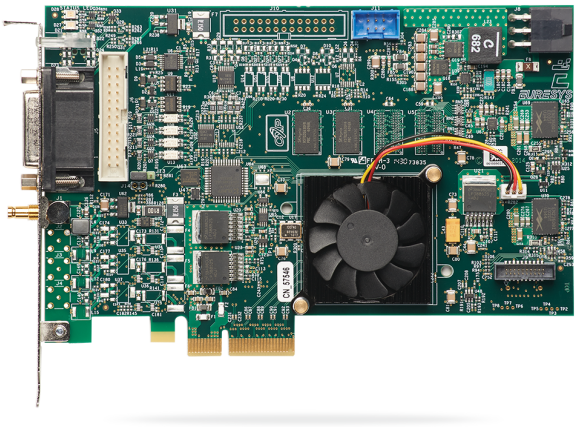
- "Mechanical Specification" on the facing page provides the product pictures, the physical dimensions, the connectors description and the pin assignments, the lamps description, etc.
- "Electrical Specification" on page 46 provides the electrical characteristics of all input/output ports, a description of the power distribution, power requirements, etc.
- "Environmental Specification" on page 74 provides the climatic requirements and CE/FCC/RoHS/WEEE compliance statements.
- "Related Products & Accessories" on page 79 provides a description of related products and accessories such as adapters, cables …

2. Mechanical Specification

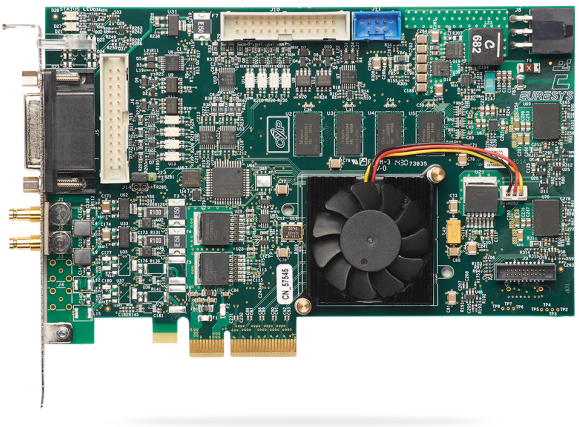
Mechanical specifications of the product(s) including: product pictures, physical dimensions, connectors description and pin assignments, lamps description, switches description, etc.

2.1. Product Pictures

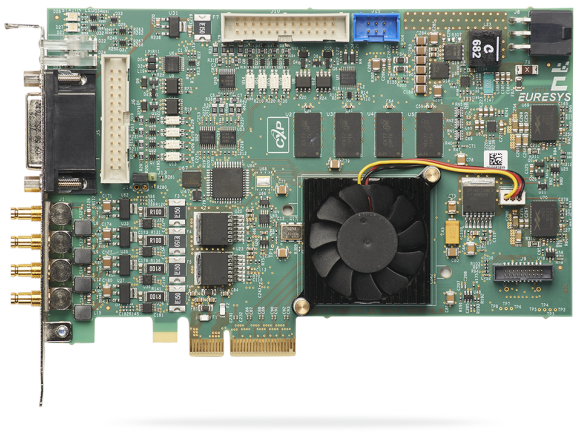
1630 Coaxlink Mono



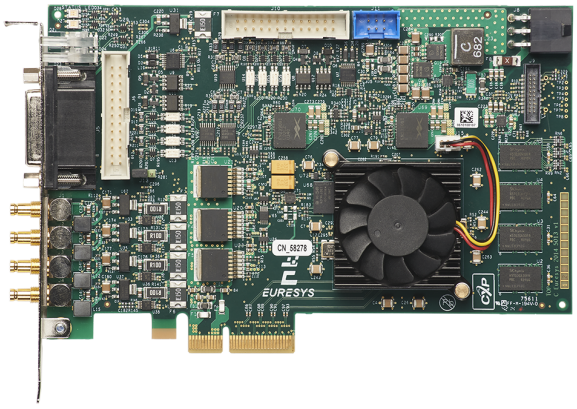
1631 Coaxlink Duo



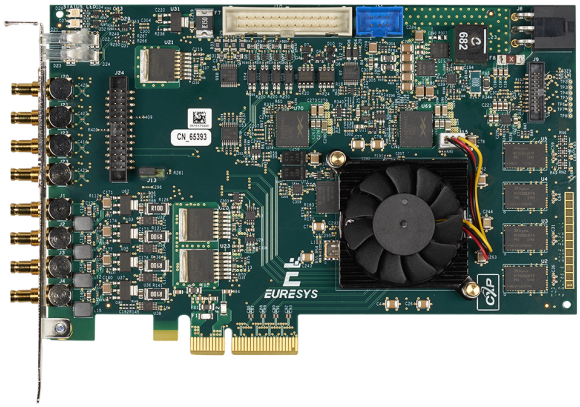
1632 Coaxlink Quad



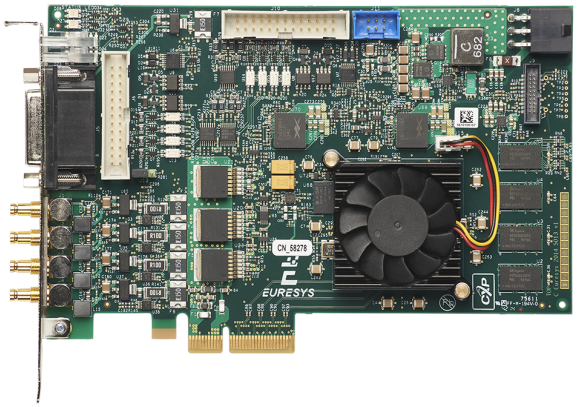
1633 Coaxlink Quad G3



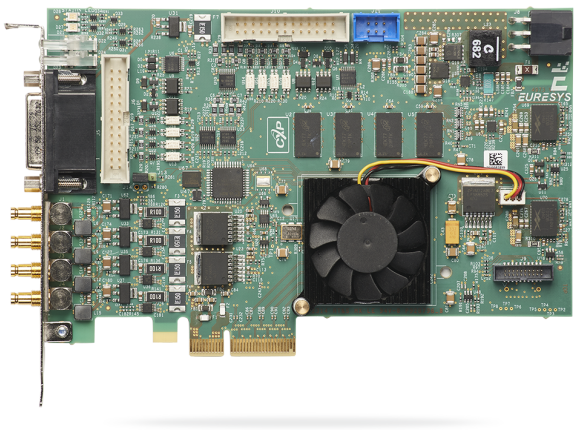
1635 Coaxlink Quad G3 DF



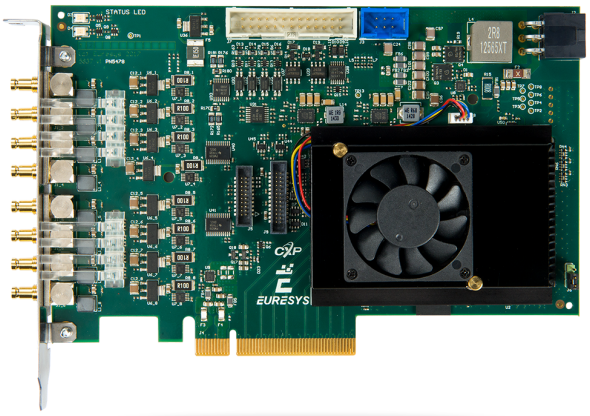
1637 Coaxlink Quad 3D-LLE



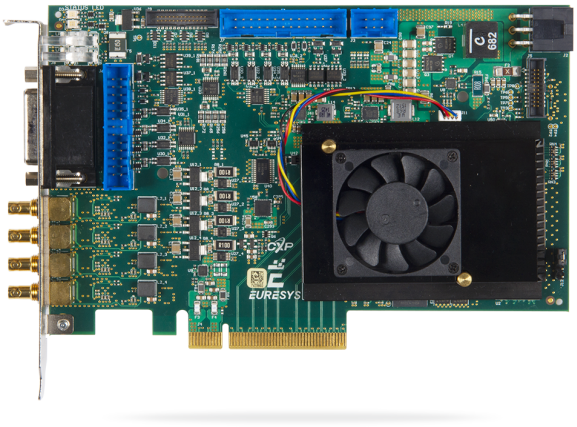
1638 Coaxlink Quad CXP-3



3602 Coaxlink Octo



3603 Coaxlink Quad CXP-12



2.2. Physical Characteristics

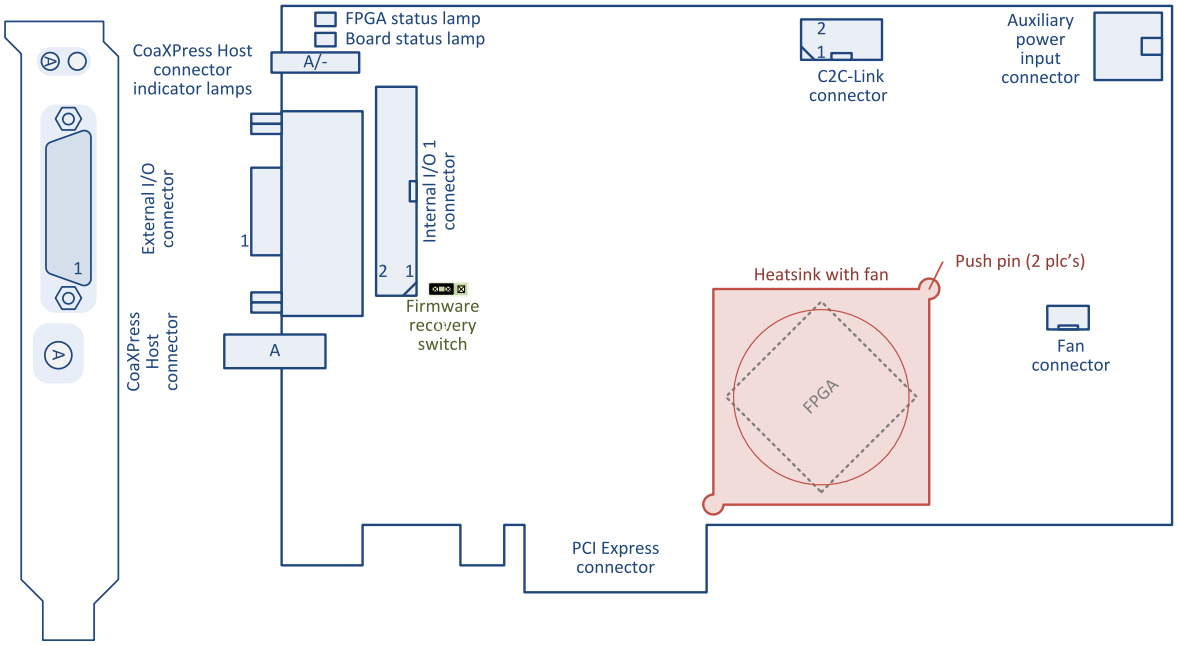
Dimensions and Weight - Coaxlink PCIe Products

Product	Length	Height	Weight
1630 Coaxlink Mono	167.65 mm, 6.6 in	111.15 mm, 4.38 in	150 g, 5.29 oz
1631 Coaxlink Duo	167.65 mm, 6.6 in	111.15 mm, 4.38 in	160 g, 5.64 oz
1632 Coaxlink Quad	167.65 mm, 6.6 in	111.15 mm, 4.38 in	170 g, 6.00 oz
1633 Coaxlink Quad G3	167.65 mm, 6.6 in	111.15 mm, 4.38 in	180 g, 6.35 oz
1635 Coaxlink Quad G3 DF	167.65 mm, 6.6 in	111.15 mm, 4.38 in	186 g, 6.56 oz
1637 Coaxlink Quad 3D-LLE	167.65 mm, 6.6 in	111.15 mm, 4.38 in	180 g, 6.35 oz
1638 Coaxlink Quad CXP-3	167.65 mm, 6.6 in	111.15 mm, 4.38 in	170 g, 6.00 oz
3602 Coaxlink Octo	167.65 mm, 6.6 in	111.15 mm, 4.38 in	189 g, 6.67 oz
3603 Coaxlink Quad CXP-12	167.65 mm, 6.6 in	111.15 mm, 4.38 in	196 g, 6.91 oz

2.3. Board and Bracket Layouts

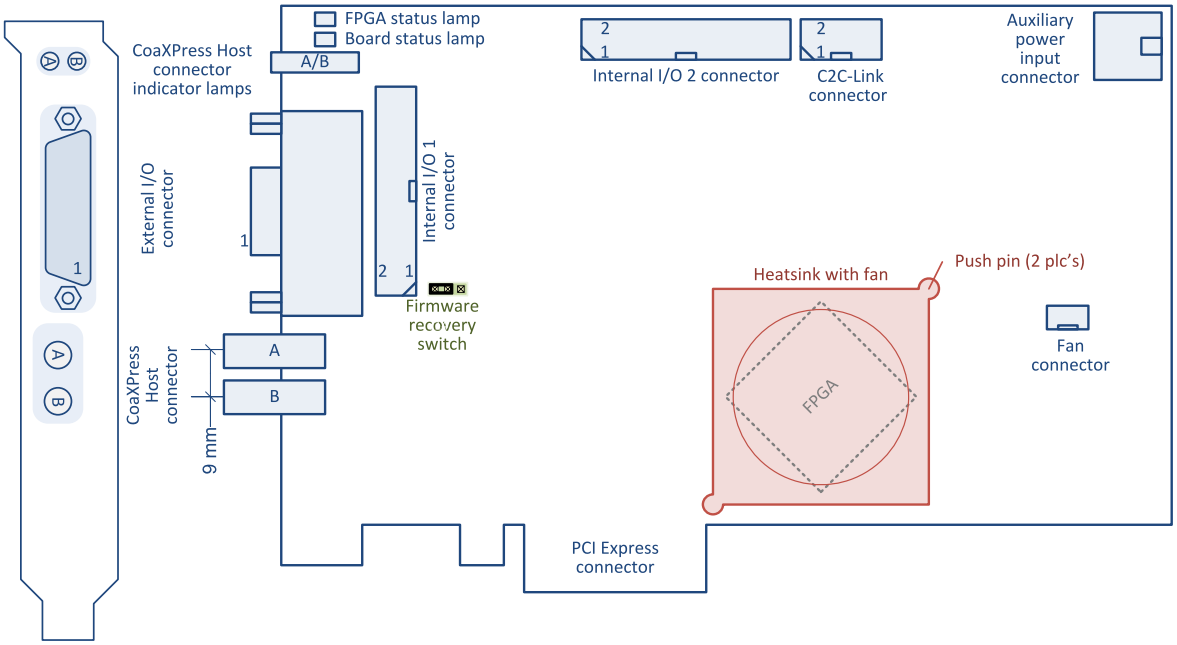
Layouts of connectors, lamps, switches and main components

1630 Coaxlink Mono



- "DIN-1 CoaXPress Host Connector" on page 22
- "External I/O Connector" on page 27
- "Internal I/O 1 Connector" on page 29
- "C2C-Link Connector" on page 39
- "Auxiliary Power Input Connector" on page 40
- "CoaXPress Lamps" on page 41
- "Board Status Lamp" on page 42
- "FPGA Status Lamp" on page 43
- "Firmware Recovery Switch" on page 44

1631 Coaxlink Duo



- "DIN-2 CoaXPress Host Connector" on page 23
- "External I/O Connector" on page 27
- "Internal I/O 1 Connector" on page 29
- "Internal I/O 2 Connector" on page 31
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- "CoaXPress Lamps" on page 41
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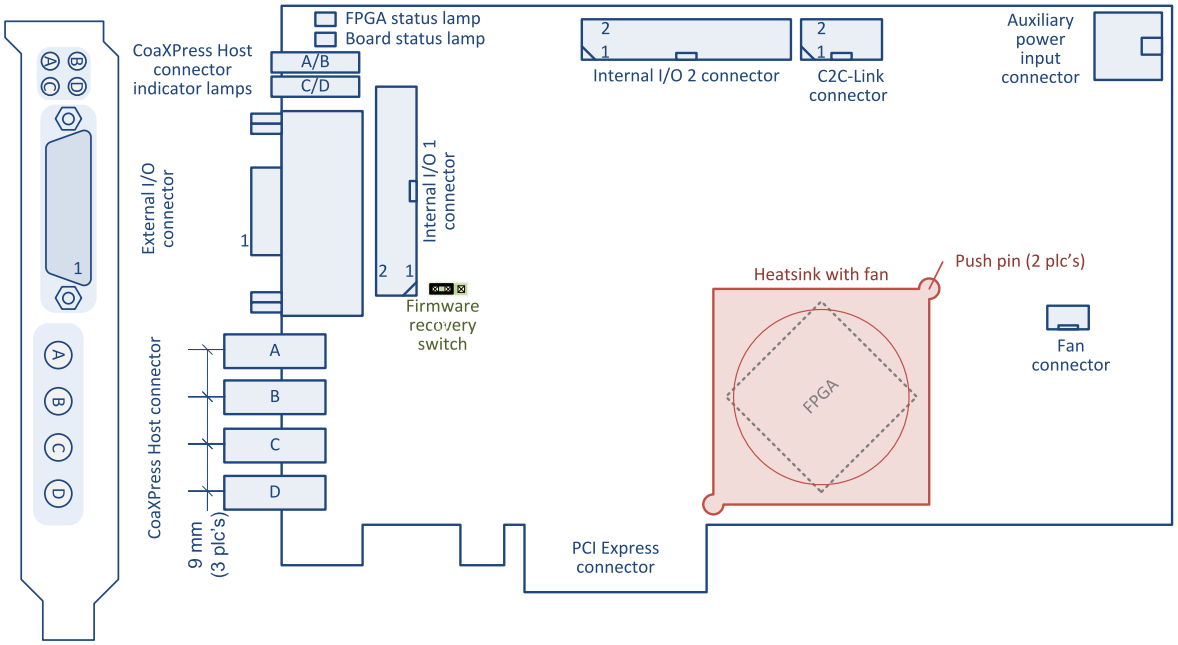
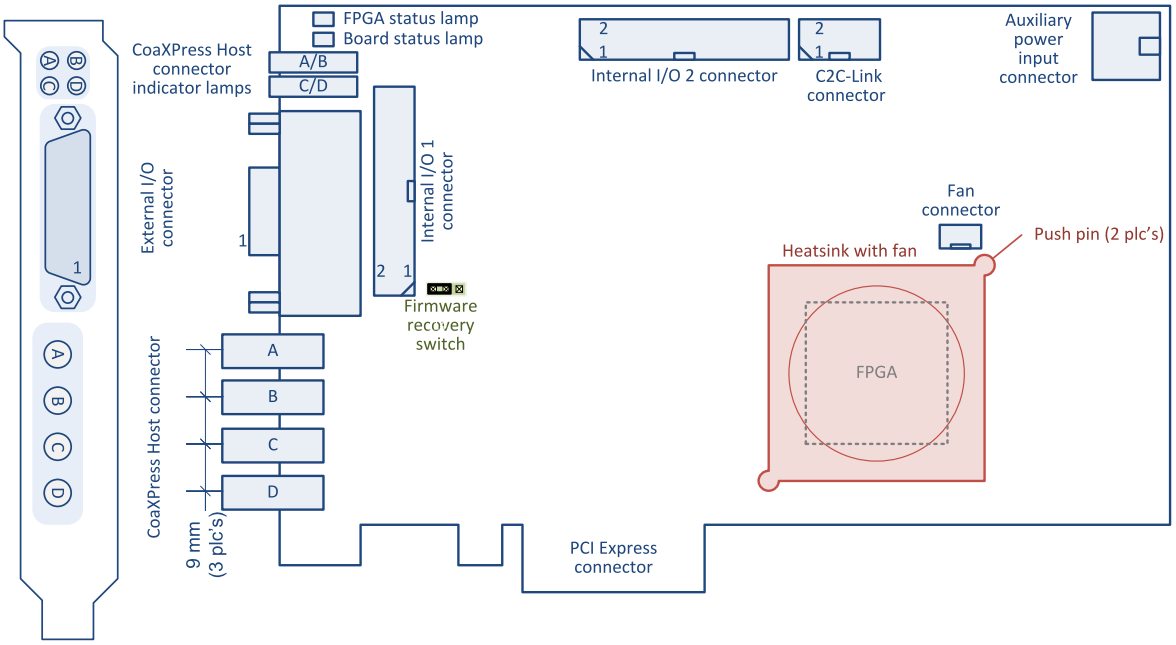
1632 Coaxlink Quad



1633 Coaxlink Quad G3



- "DIN-4 CoaXPress Host Connector" on page 24
- "External I/O Connector" on page 27
- "Internal I/O 1 Connector" on page 29
- "Internal I/O 2 Connector" on page 31
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- "CoaXPress Lamps" on page 41
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- "FPGA Status Lamp" on page 43
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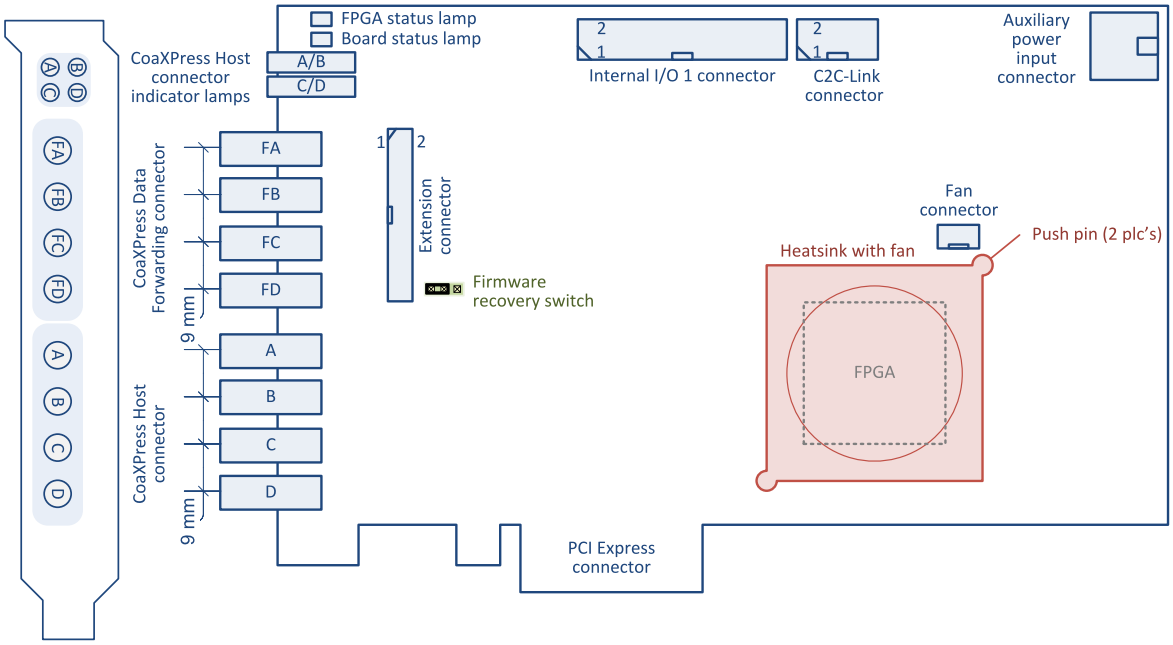
1635 Coaxlink Quad G3 DF



- "DIN-4 CoaXPress Host Connector" on page 24
- "CoaXPress Data Forwarding Connector" on page 25
- "Internal I/O 1 Connector" on page 29
- "C2C-Link Connector" on page 39
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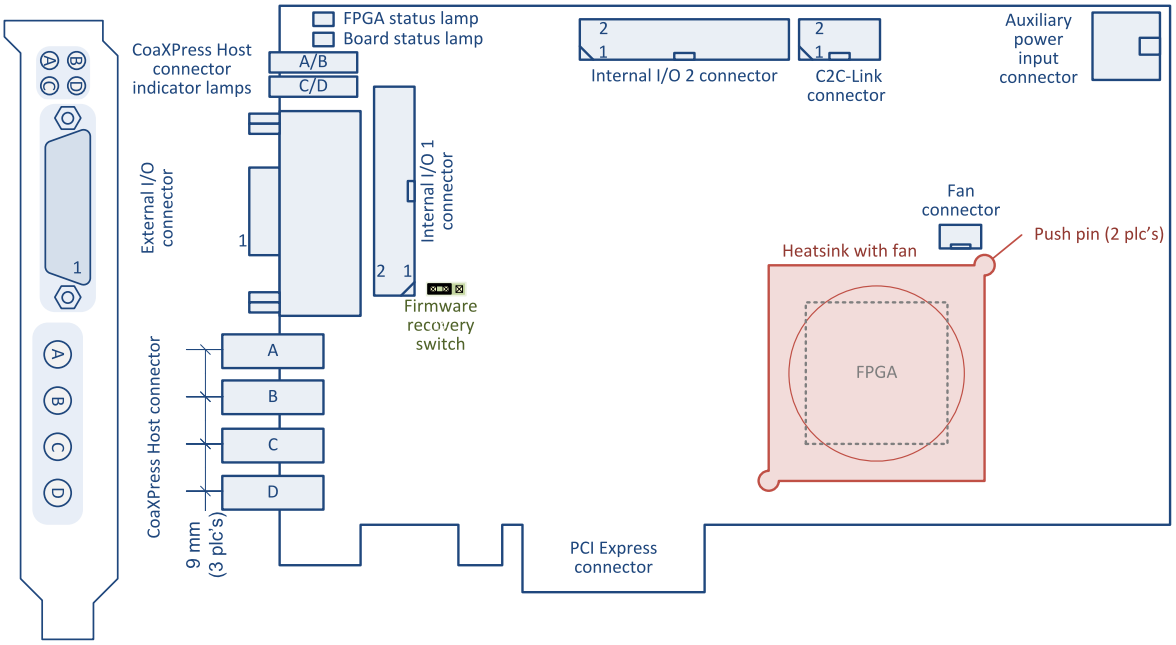
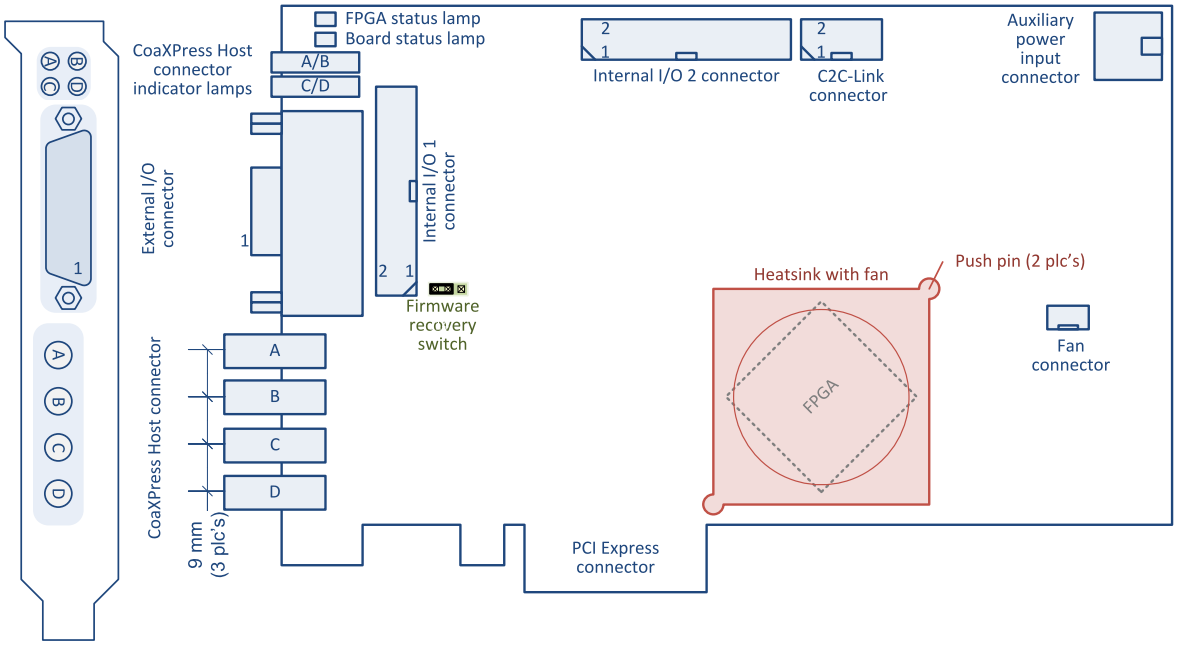
1637 Coaxlink Quad 3D-LLE



1638 Coaxlink Quad CXP-3



- "DIN-4 CoaXPress Host Connector" on page 24
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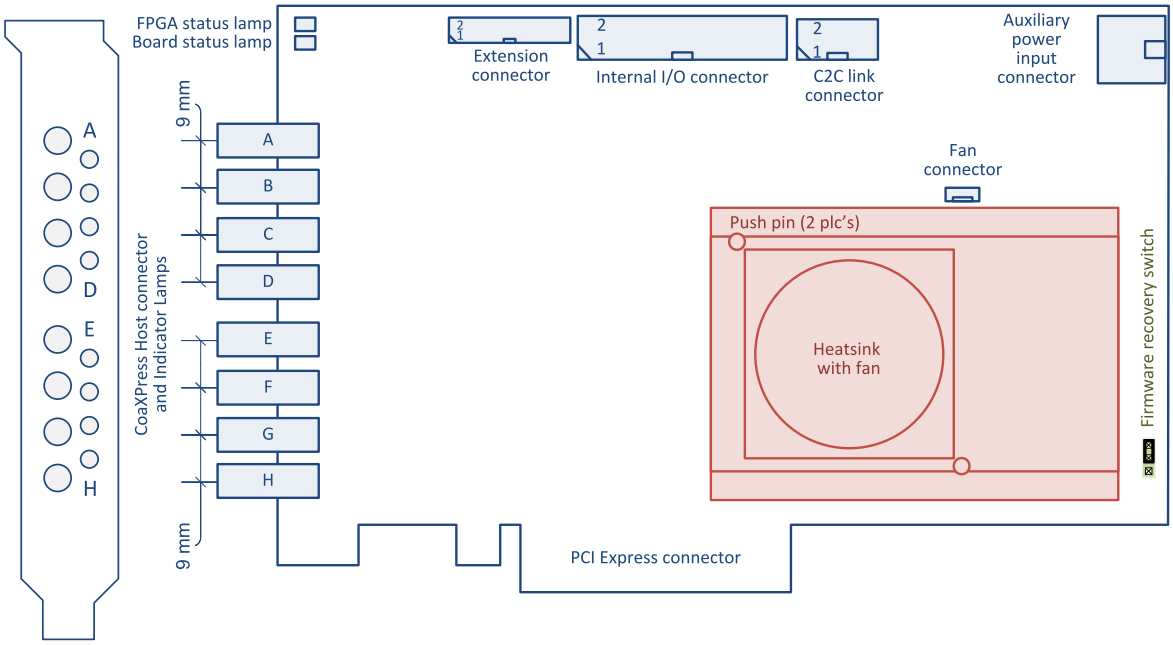
- "Firmware Recovery Switch" on page 44

3602 Coaxlink Octo



- "DIN-8 CoaXPress Host Connector" on page 26
- "Internal I/O 1 Connector" on page 29
- "C2C-Link Connector" on page 39
- "Auxiliary Power Input Connector" on page 40
- "CoaXPress Lamps" on page 41
- "Board Status Lamp" on page 42
- "FPGA Status Lamp" on page 43
- "Firmware Recovery Switch" on page 44

3603 Coaxlink Quad CXP-12

TBD

2.4. Connectors

DIN-1 CoaXPress Host Connector

Applies to: Mono

Connector description

Property	Value
Name	DIN-1 CoaXPress Host
Type	DIN 1.0/2.3 75 Ohms coaxial female receptacle
Location	Card bracket
Usage	CoaXPress Host Interface CoaXPress Data Forwarding Interface

Pin assignments

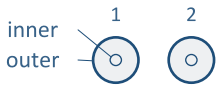
Pin	Signal	Usage
Inner	CXP_A	CoaXPress Host Connection A
Outer	GND	Ground

DIN-2 CoaXPress Host Connector

Applies to: Duo

Connector description

Property	Value
Name	DIN-2 CoaXPress Host
Type	2 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Host Interface CoaXPress Data Forwarding Interface



Pin assignments

Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground

DIN-4 CoaXPress Host Connector

Applies to: Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE

Connector description

Property	Value
Name	DIN-4 CoaXPress Host
Type	4 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Host Interface CoaXPress Data Forwarding Interface

Pin assignments

Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground
Inner3	CXP_C	CoaXPress Host Connection C
Outer3	GND	Ground
Inner4	CXP_D	CoaXPress Host Connection D
Outer4	GND	Ground

CoaXPress Data Forwarding Connector

Applies to: QuadG3DF

Connector description

Property	Value
Name	CoaXPress Data Forwarding
Type	4 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Card bracket
Usage	

Pin assignments

Pin	Signal	Usage
Inner1	CXP_FA	CoaXPress Data Forwarding Connection A
Outer1	GND	Ground
Inner2	CXP_FB	CoaXPress Data Forwarding Connection B
Outer2	GND	Ground
Inner3	CXP_FC	CoaXPress Data Forwarding Connection C
Outer3	GND	Ground
Inner4	CXP_FD	CoaXPress Data Forwarding Connection D
Outer4	GND	Ground

DIN-8 CoaXPress Host Connector

Applies to: Octo

Connector description

Property	Value
Name	DIN-8 CoaXPress Host
Type	8 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Host Interface CoaXPress Data Forwarding Interface

Pin assignments

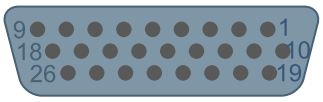
Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground
Inner3	CXP_C	CoaXPress Host Connection C
Outer3	GND	Ground
Inner4	CXP_D	CoaXPress Host Connection D
Outer4	GND	Ground
Inner5	CXP_E	CoaXPress Host Connection E
Outer5	GND	Ground
Inner6	CXP_F	CoaXPress Host Connection F
Outer6	GND	Ground
Inner7	CXP_G	CoaXPress Host Connection G
Outer7	GND	Ground
Inner8	CXP_H	CoaXPress Host Connection H
Outer8	GND	Ground

External I/O Connector

Applies to: Mono Duo Quad QuadG3 QuadCXP3 Quad3DLLE

Connector description

Property	Value
Name	External I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN12+	High-speed differential input #12 – Positive pole
3	IIN11+	Isolated input #11 – Positive pole
4	IIN13-	Isolated input #13 – Negative pole
5	IIN14-	Isolated input #14 – Negative pole
6	IOUT12-	Isolated contact output #12 – Negative pole
7	GND	Ground
8		Not connected
9	GND	Ground
10	GND	Ground
11	DIN12-	High-speed differential input #12 – Negative pole
12	IIN11-	Isolated input #11 – Negative pole
13	IIN12+	Isolated input #12 – Positive pole
14	IIN13+	Isolated input #13 – Positive pole
15	IIN14+	Isolated input #14 – Positive pole

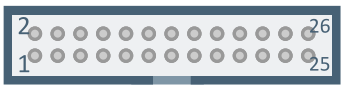
Pin	Signal	Usage
16	IOUT12+	Isolated contact output #12 – Positive pole
17	TTLIO12	TTL input/output #12
18	GND	Ground
19	DIN11-	High-speed differential input #11 – Negative pole
20	DIN11+	High-speed differential input #11 – Positive pole
21	IIN12-	Isolated input #12 – Negative pole
22	IOUT11-	Isolated contact output #11 – Negative pole
23	IOUT11+	Isolated contact output #11 – Positive pole
24	GND	Ground
25	TTLIO11	TTL input/output #11
26	+12V	+12 V Power output

Internal I/O 1 Connector

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo

Connector description

Property	Value
Name	Internal I/O 1
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN11+	High-speed differential input #11 – Positive pole
4	DIN11-	High-speed differential input #11 – Negative pole
5	DIN12+	High-speed differential input #12 – Positive pole
6	DIN12-	High-speed differential input #12 – Negative pole
7	IIN11+	Isolated input #11 – Positive pole
8	IIN11-	Isolated input #11 – Negative pole
9	IIN12+	Isolated input #12 – Positive pole
10	IIN12-	Isolated input #12 – Negative pole
11	IIN13+	Isolated input #13 – Positive pole
12	IIN13-	Isolated input #13 – Negative pole
13	IIN14+	Isolated input #14 – Positive pole
14	IIN14-	Isolated input #14 – Negative pole
15	IOUT11+	Isolated contact output #11 – Positive pole

Pin	Signal	Usage
16	IOUT11-	Isolated contact output #11 – Negative pole
17	IOUT12+	Isolated contact output #12 – Positive pole
18	IOUT12-	Isolated contact output #12 – Negative pole
19	TTLIO11	TTL input/output #11
20	GND	Ground
21	TTLIO12	TTL input/output #12
22	GND	Ground
23		Not connected
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

Internal I/O 2 Connector

Applies to: Duo Quad QuadG3 QuadCXP3 Quad3DLLE

Connector description

Property	Value
Name	Internal I/O 2
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output

Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN21+	High-speed differential input #21 – Positive pole
4	DIN21-	High-speed differential input #21 – Negative pole
5	DIN22+	High-speed differential input #22 – Positive pole
6	DIN22-	High-speed differential input #22 – Negative pole
7	IIN21+	Isolated input #21 – Positive pole
8	IIN21-	Isolated input #21 – Negative pole
9	IIN22+	Isolated input #22 – Positive pole
10	IIN22-	Isolated input #22 – Negative pole
11	IIN23+	Isolated input #23 – Positive pole
12	IIN23-	Isolated input #23 – Negative pole
13	IIN24+	Isolated input #24 – Positive pole
14	IIN24-	Isolated input #24 – Negative pole
15	IOUT21+	Isolated contact output #21 – Positive pole

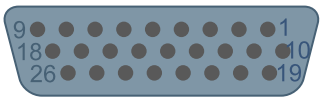
Pin	Signal	Usage
16	IOUT21-	Isolated contact output #21 – Negative pole
17	IOUT22+	Isolated contact output #22 – Positive pole
18	IOUT22-	Isolated contact output #22 – Negative pole
19	TTLIO21	TTL input/output #21
20	GND	Ground
21	TTLIO22	TTL input/output #22
22	GND	Ground
23		Not connected
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

Remote External I/O Connector

Applies to: Octo QuadCXP12

Connector description

Property	Value
Name	Remote External I/O
Type	26-pin 3-row high-density female sub-D connector
Location	3610/3612 I/O extension module bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
26	+12V	+12 V Power output
20	IO01_DIO01+	Single-ended I/O #1 or differential I/O #1 positive pole
19	IO02_DIO01-	Single-ended I/O #2 or differential I/O #1 negative pole
2	IO03_DIO02+	Single-ended I/O #3 or differential I/O #2 positive pole
11	IO04_DIO02-	Single-ended I/O #4 or differential I/O #2 negative pole
3	IO05_DIO03+	Single-ended I/O #5 or differential I/O #3 positive pole
12	IO06_DIO03-	Single-ended I/O #6 or differential I/O #3 negative pole
13	IO07_DIO04+	Single-ended I/O #7 or differential I/O #4 positive pole
21	IO08_DIO04-	Single-ended I/O #8 or differential I/O #4 negative pole
15	IO09_DIO05+	Single-ended I/O #9 or differential I/O #5 positive pole
5	IO10_DIO05-	Single-ended I/O #10 or differential I/O #5 negative pole
23	IO11_DIO06+	Single-ended I/O #11 or differential I/O #6 positive pole
22	IO12_DIO06-	Single-ended I/O #12 or differential I/O #6 negative pole
16	IO13_DIO07+	Single-ended I/O #13 or differential I/O #7 positive pole
6	IO14_DIO07-	Single-ended I/O #14 or differential I/O #7 negative pole

Pin	Signal	Usage
25	IO15_DIO08+	Single-ended I/O #15 or differential I/O #8 positive pole
24	IO16_DIO08-	Single-ended I/O #16 or differential I/O #8 negative pole
17	IO17_DIO09+	Single-ended I/O #17 or differential I/O #9 positive pole
7	IO18_DIO09-	Single-ended I/O #18 or differential I/O #9 negative pole
9	IO19_DIO10+	Single-ended I/O #19 or differential I/O #10 positive pole
18	IO20_DIO10-	Single-ended I/O #20 or differential I/O #10 negative pole
1	GND	Ground
4	GND	Ground
8	GND	Ground
10	GND	Ground
14	GND	Ground

Remote Internal I/O Connector

Applies to: Octo QuadCXP12

Connector description

Property	Value
Name	Remote Internal I/O
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	3610/3612 I/O extension module card
Usage	General purpose I/O and power output

Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	IO01_DIO01+	Single-ended I/O #1 or differential I/O #1 positive pole
4	IO02_DIO01-	Single-ended I/O #2 or differential I/O #1 negative pole
5	IO03_DIO02+	Single-ended I/O #3 or differential I/O #2 positive pole
6	IO04_DIO02-	Single-ended I/O #4 or differential I/O #2 negative pole
7	IO05_DIO03+	Single-ended I/O #5 or differential I/O #3 positive pole
8	IO06_DIO03-	Single-ended I/O #6 or differential I/O #3 negative pole
9	IO07_DIO04+	Single-ended I/O #7 or differential I/O #4 positive pole
10	IO08_DIO04-	Single-ended I/O #8 or differential I/O #4 negative pole
11	GND	Ground
12	GND	Ground
13	IO09_DIO05+	Single-ended I/O #9 or differential I/O #5 positive pole
14	IO10_DIO05-	Single-ended I/O #10 or differential I/O #5 negative pole
15	IO11_DIO06+	Single-ended I/O #11 or differential I/O #6 positive pole

Pin	Signal	Usage
16	IO12_DIO06-	Single-ended I/O #12 or differential I/O #6 negative pole
17	IO13_DIO07+	Single-ended I/O #13 or differential I/O #7 positive pole
18	IO14_DIO07-	Single-ended I/O #14 or differential I/O #7 negative pole
19	IO15_DIO08+	Single-ended I/O #15 or differential I/O #8 positive pole
20	IO16_DIO08-	Single-ended I/O #16 or differential I/O #8 negative pole
21	IO17_DIO09+	Single-ended I/O #17 or differential I/O #9 positive pole
22	IO18_DIO09-	Single-ended I/O #18 or differential I/O #9 negative pole
23	IO19_DIO10+	Single-ended I/O #19 or differential I/O #10 positive pole
24	IO20_DIO10-	Single-ended I/O #20 or differential I/O #10 negative pole
25	+12V	+12 V Power output
26	+12V_RTN	Ground

I/O Extension Connector

Applies to: Octo QuadCXP12

Connector description

Property	Value
Name	I/O Extension
Type	26-pin dual-row 0.050" pitch pin header with shrouding
Location	
Usage	I/O extension

Pin assignments

Pin	Signal	Usage
1		1-wire serial I/O
2	GND	Ground
3	IOEXT01	IO Extension #1
4	+3V3	+3.3 V Power
5	IOEXT02	IO Extension #2
6	GND	Ground
7	IOEXT03	IO Extension #3
8	+3V3	+3.3 V Power
9	IOEXT04	IO Extension #4
10	GND	Ground
11	IOEXT05	IO Extension #5
12	+3V3	+3.3 V Power
13	IOEXT06	IO Extension #6
14	GND	Ground
15	IOEXT07	IO Extension #7

Pin	Signal	Usage
16	+3V3	+3.3 V Power
17	IOEXT08	IO Extension #8
18	GND	Ground
19	IOEXT09	IO Extension #9
20	12V	12V Power
21	IOEXT10	IO Extension #10
22	GND	Ground
23	IOEXT11	IO Extension #11
24	12V	12V Power
25	IOEXT12	IO Extension #12
26	GND	Ground

C2C-Link Connector

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo

Connector description

Property	Value
Name	C2C-Link
Type	6-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	Card-to-card link

Pin assignments

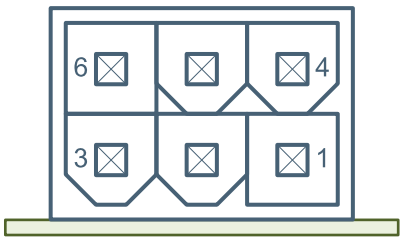
Pin	Signal	Usage
1	GND	Ground
2	CSync1	Card-to-card synchronization bus – Signal 1
3	GND	Ground
4	CSync2	Card-to-card synchronization bus – Signal 2
5	GND	Ground
6	CSync3	Card-to-card synchronization bus – Signal 3

Auxiliary Power Input Connector

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo

Connector description

Property	Value
Name	Auxiliary Power Input
Type	6-pin PCI Express x16 Graphics 150W ATX power socket connector
Location	Printed circuit board
Usage	DC power input for PoCXP and GPIO power output



Pin assignments

Pin	Signal	Usage
1	+12VIN	Auxiliary +12 V input
2	+12VIN	Auxiliary +12 V input
3	+12VIN	Auxiliary +12 V input
4	GND	Ground
5	SenseIN	Power source presence detection
6	GND	Ground

2.5. Lamps

CoaXPress Lamps

Each connector of the CoaXPress Host Interface is associated with a *CoaXPress Host Indicator Lamp* that indicates the state of the CoaXPress Link connection.

CoaXPress Host Connector Indicator Lamps State

Symbol	Lamp State	Meaning
	Off	The Coaxlink card is not powered
	Solid orange	System booting
	Fast flash alternate green / orange	The connection detection is in progress; PoCXP is active. *This state is shown for a minimum of 1s even if the connection detection is faster*
	Fast flash orange	The connection detection is in progress; PoCXP is off. *This state is shown for a minimum of 1s even if the connection detection is faster*
	Solid red	The PoCXP over-current protection has tripped.
	Solid green	The Device to Host connection is established, but no data being transferred
	Slow pulse orange	The Device to Host connection is established, but the Host is waiting for a trigger.
	Fast flash green.	The Device to Host connection is established and image data is being transferred

Flashing Lamp States Timing Definitions

Indication	Timing
Fast flash	**12.5Hz @25% duty cycle**: 20 ms on, 60 ms off
Fast flash alternate (color 1/color 2)	**12.5Hz @25% duty cycle**: 20 ms on (color 1), 60 ms off, 20 ms on (color 2), 60 ms off
Slow flash	**0.5Hz @50% duty cycle**: 1 second on, 1 second off
Slow pulse (red | orange)	**1Hz @ 20% duty cycle:** 200ms on, 800ms off

Board Status Lamp

Board status lamp indicator states

Lamp state	Symbol	Meaning
Off		**No power.** The board is not powered or the power distribution network is not functional.
Solid green		**Board status OK.** The main power distribution network is operational and the FPGA start-up procedure has successfully completed.
Solid red		**Board status NOK.** Possible causes are: • There is no power delivered on the +12 V rail of the PCI Express connector slot • The FPGA start-up procedure is not completed. *The normal completion time is around 100 milliseconds.* • At least one power converter of the main power distribution network is unable to operate properly. *This might be caused by excessive temperature due to inadequate board cooling, accidental short-circuits having blown one (or more) protection fuses, inappropriate supply voltages, etc.*

FPGA Status Lamp

FPGA status lamp indicator states

Lamp state	Symbol	Meaning
Off		**Board not powered.**
Solid green		**FPGA status OK.** All the FPGA clock networks and the DDR memory are operating normally.
Solid red		**FPGA status NOK.** Possible causes are: • At least one FPGA clock network is not operating normally. *This might be caused by excessive jitter on external clock signals of the CoaXPress or the PCI Express interfaces.* • The DDR memory controller has not been able to successfully perform the calibration procedure.

2.6. Firmware Recovery Switch

The firmware recovery switch is implemented with a 3-pin 1-row header and a jumper. The jumper has two positions: **normal** and **recovery**.

Normal position

At the next power ON, the latest firmware successfully written into the Flash EEPROM is used to program the FPGA.

After FPGA startup completion, the card exhibits the standard PCI ID and the Coaxlink driver allows normal operation.

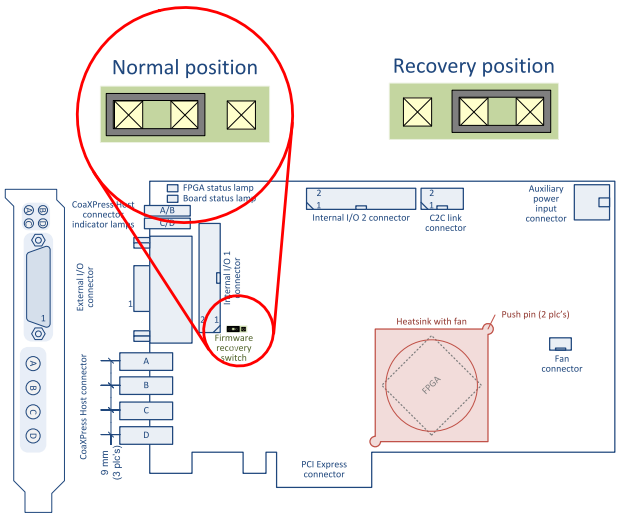
This is the factory default jumper position.

Recovery position

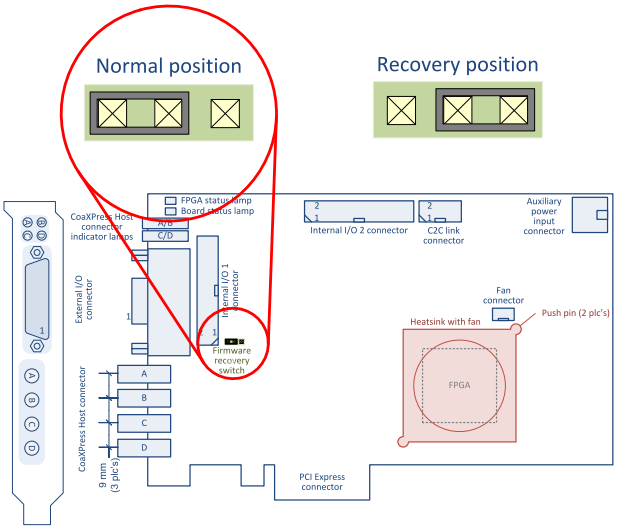
At the next power ON, the last but one firmware successfully written into the Flash EEPROM is used to program the FPGA.

After FPGA startup completion, the card exhibits the recovery PCI ID and the Coaxlink driver inhibits image acquisition.

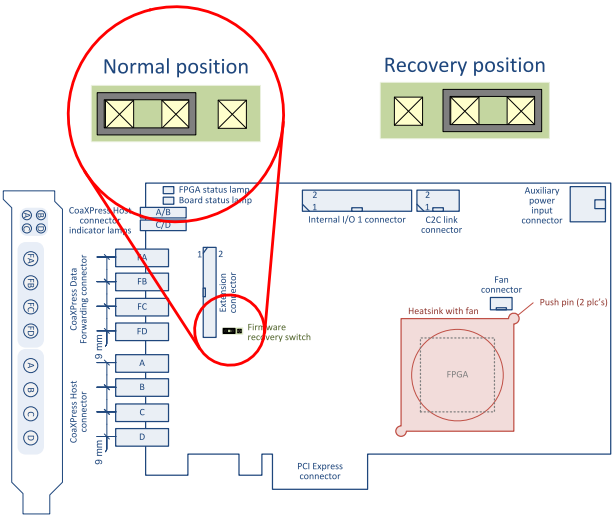
1632 Coaxlink Quad



1633 Coaxlink Quad G3, 1633-LH Coaxlink Quad G3 LH, 1637 Coaxlink Quad 3D-LLE



1635 Coaxlink Quad G3 DF, 3601 Coaxlink CoaXPress Simulator



Note: *The normal position of the jumper (i.e. bracket side) is common to all Coaxlink PCI Express cards.*

3. Electrical Specification

Electrical specification of the product(s) including: electrical characteristics of all the input/output ports, description of the power distribution, power requirements, etc.

3.1. CoaXPress Host Interface

Electrical specification of the CoaXPress Host interface

CoaXPress Host Interface Type per Product

Each connection of the CoaXPress Host interface implements a **Host Transceiver** (HT) and a **Power Transmitting Unit** (PTU).

Product	HT Type
1630 Coaxlink Mono	"CXP-12 Host Transceiver (Preliminary)" below
1631 Coaxlink Duo	"CXP-12 Host Transceiver (Preliminary)" below
1632 Coaxlink Quad	"CXP-12 Host Transceiver (Preliminary)" below
1633 Coaxlink Quad G3	"CXP-12 Host Transceiver (Preliminary)" below
1635 Coaxlink Quad G3 DF	"CXP-12 Host Transceiver (Preliminary)" below
1637 Coaxlink Quad 3D-LLE	"CXP-12 Host Transceiver (Preliminary)" below
1638 Coaxlink Quad CXP-3	"CXP-3 Host Transceiver" on the next page
3602 Coaxlink Octo	"CXP-12 Host Transceiver (Preliminary)" below

CXP-12 Host Transceiver (Preliminary)

Applies to: QuadCXP12

The Host transceiver implements a **high-speed cable receiver** and a **low-speed cable driver** for **CXP-12** speeds.

It fulfills the electrical specification of the CoaXPress 2.0 standard. Namely:

- The cable receiver requirements for the high-speed connection described in TBD
- The cable driver requirements for the low-speed connection described in TBD

Host Transceiver Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
High-speed connection bit rate		1.25		12.50	GT/s
Low-speed connection bit rate	1.25 GT/s up to 6.25 GT/s		20.833		MT/s
	10.0 GT/s and 12.5 GT/S		41.666		MT/s

Parameter	Conditions	Min.	Typ.	Max.	Unit
Max. cable length	BELDEN 1694 @ 1.25 GT/s	TBD			m
	BELDEN 1694 @ 2.5 GT/s	TBD			m
	BELDEN 1694 @ 3.125 GT/s	TBD			m
	BELDEN 1694 @ 5 GT/s	TBD			m
	BELDEN 1694 @ 6.25 GT/s	TBD			m
	BELDEN 1694 @ 10.0 GT/s	TBD			m
	BELDEN 1694 @ 6.25 GT/s	TBD			m

CXP-6 Host Transceiver

Applies to: Mono Duo Quad QuadG3 QuadG3DF Quad3DLLE Octo

The Host transceiver implements a **high-speed cable receiver** and a **low-speed cable driver** for **CXP-6** speeds.

It fulfills the electrical specification of the CoaXPress 1.1 standard. Namely:

- The cable receiver requirements for the high-speed connection described in Table 2 of the Annex B of the CoaXPress Standard 1.1
- The cable driver requirements for the low-speed connection described in Table 3 of the Annex B of the CoaXPress Standard 1.1

Host Transceiver Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
High-speed connection bit rate		1.25		6.25	GT/s
Low-speed connection bit rate			20.833		MT/s
Max. cable length	BELDEN 1694 @ 1.25 GT/s	130			m
	BELDEN 1694 @ 2.5 GT/s	110			m
	BELDEN 1694 @ 3.125 GT/s	100			m
	BELDEN 1694 @ 5 GT/s	60			m
	BELDEN 1694 @ 6.25 GT/s	40			m

CXP-3 Host Transceiver

Applies to: QuadCXP3

The Host transceiver implements a **high-speed cable receiver** and a **low-speed cable driver** for **CXP-3** speeds.

It fulfills the electrical specification of the CoaXPress 1.1 standard. Namely:

- The cable receiver requirements for the high-speed connection described in Table 2 of the Annex B of the CoaXPress Standard 1.1
- The cable driver requirements for the low-speed connection described in Table 3 of the Annex B of the CoaXPress Standard 1.1

Host Transceiver Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
High-speed connection bit rate		1.25		3.125	GT/s
Low-speed connection bit rate			20.833		MT/s
Max. cable length	BELDEN 1694 @ 1.25 GT/s	130			m
	BELDEN 1694 @ 2.5 GT/s	110			m
	BELDEN 1694 @ 3.125 GT/s	100			m

Power Transmitting Unit

The Power Transmitting Unit implements Power over CoaXPress (PoCXP) as specified in section 7 of the CoaXPress Standard 1.1.

If fulfills all the requirements for a Host; namely:

- Over-current protection (OCP)
- PoCXP CoaXPress Device detection

In addition: it provides the user with an AUTO/OFF control:

- Setting the control to AUTO initiates a new PoCXP device detection; the power will be applied only if the detection succeeds
- Setting the control to OFF forces the PTU to disconnect. *The control is OFF after power on, and, if providing power to the camera is required, has to be set to AUTO by the application.*

Power Transmitting Unit Specification

Parameter	Min.	Typ.	Max.	Unit
DC output voltage	22	24	26	V
Available output power	17			W
OCP holding current	790			mA
OCP nominal trip current			5	A
PoCXP Device detection sensing current	550		1,000	µA

Note: *The above specification applies over the whole operating temperature range of the Coaxlink card.*

3.2. PCI Express Interface

Specification of the PCI Express Interface

The PCI Express Interface implements a **PCIe end-point** interface and provides **electrical power** to the Coaxlink card.

PCI Express End-point Type per Product

Product	Type
1630 Coaxlink Mono	"4-lane Rev 2.0 PCIe End-point" on page 54
1631 Coaxlink Duo	"4-lane Rev 2.0 PCIe End-point" on page 54
1632 Coaxlink Quad	"4-lane Rev 2.0 PCIe End-point" on page 54
1633 Coaxlink Quad G3	"4-lane Rev 3.0 PCIe End-point " on page 53
1635 Coaxlink Quad G3 DF	"4-lane Rev 3.0 PCIe End-point " on page 53
1637 Coaxlink Quad 3D-LLE	"4-lane Rev 2.0 PCIe End-point" on page 54
1638 Coaxlink Quad CXP-3	"4-lane Rev 2.0 PCIe End-point" on page 54
3602 Coaxlink Octo	"8-lane Rev 3.0 PCIe End-point" on the next page

8-lane Rev 3.0 PCIe End-point

Applies to: Octo

The 8-lane Rev 3.0 PCIe end-point:

- complies with Revision 3.0 of the PCI Express Card Electromechanical specification.
- supports 1-lane, 2-lane, 4-lane and 8-lane link width
- supports PCIe Rev 3.0 link speed (8.0 GT/s with 128b/130b coding)
- supports PCIe Rev 2.0 link speed (5.0 GT/s with 8b/10b coding)
- supports the PCIe Rev 1.0 link speed (2.5 GT/s with 8b/10b coding)
- supports payload size up to 512 bytes
- offers the optimal performance when it is configured for 8-lane PCIe Rev 3.0 link speed (8 GT/s)

8-lane Rev 3.0 PCIe end-point to PC memory data transfer performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	8-lane @ 8 GT/s (PCIe Rev 3.0)		6,700		MB/s
	8-lane @ 5 GT/s (PCIe Rev 2.0)		3,400		MB/s
	4-lane @ 8 GT/s (PCIe Rev 3.0)		3,350		MB/s
	4-lane @ 5 GT/s (PCIe Rev 2.0)		1,700		MB/s
	2-lane @ 8 GT/s (PCIe Rev 3.0)		1,700		MB/s
	2-lane @ 5 GT/s (PCIe Rev 2.0)		800		MB/s
	1-lane @ 8 GT/s (PCIe Rev 3.0)		800		MB/s

4-lane Rev 3.0 PCIe End-point

Applies to: QuadG3 QuadG3DF

The 4-lane Rev 3.0 PCIe end-point:

- complies with Revision 3.0 of the PCI Express Card Electromechanical specification.
- supports 1-lane, 2-lane, and 4-lane link width
- supports PCIe Rev 3.0 link speed (8.0 GT/s with 128b/130b coding)
- supports PCIe Rev 2.0 link speed (5.0 GT/s with 8b/10b coding)
- **doesn't support** the PCIe Rev 1.0 link speed (2.5 GT/s with 8b/10b coding)
- supports payload size up to 512 bytes
- offers the optimal performance when it is configured for 4-lane PCIe Rev 3.0 link speed (8 GT/s)

4-lane Rev 3.0 PCIe end-point to PC memory data transfer performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	4-lane @ 8 GT/s (PCIe Rev 3.0)		3,350		MB/s
	4-lane @ 5 GT/s (PCIe Rev 2.0)		1,700		MB/s
	2-lane @ 8 GT/s (PCIe Rev 3.0)		1,700		MB/s
	2-lane @ 5 GT/s (PCIe Rev 2.0)		800		MB/s
	1-lane @ 8 GT/s (PCIe Rev 3.0)		800		MB/s

4-lane Rev 2.0 PCIe End-point

Applies to: Mono Duo Quad QuadCXP3 Quad3DLLE QuadCXP12

The 4-lane Rev 2.0 PCIe end-point:

- complies with Revision 2.0 of the PCI Express Card Electromechanical specification.
- supports 1-lane, 2-lane, and 4-lane link width
- supports PCIe Rev 2.0 link speed (5.0 GT/s with 8b/10b coding)
- supports PCIe Rev 1.0 link speed (2.5 GT/s with 8b/10b coding)
- supports payload size up to 512 bytes
- offers the optimal performance when it is configured for 4-lane PCIe Rev 2.0 link speed (5 GT/s)

4-lane Rev 3.0 PCIe end-point to PC memory data transfer performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	4-lane @ 5 GT/s (PCIe Rev 2.0)		1,700		MB/s
	4-lane @ 2.5 GT/s (PCIe Rev 1.0)		800		MB/s
	2-lane @ 5 GT/s (PCIe Rev 2.0)		800		MB/s

3.3. Power Distribution

Description of the power distribution

Power Distribution Schemes of PCIe Products

The power distribution scheme of a Coaxlink PCIe product has two distinct distribution networks:

- The main power distribution network
- The auxiliary power distribution network

PCIe Products - Main power distribution network

The main power distribution network delivers power to **all the on-board electronic devices** including FPGA, memory chips, CoaXPress transceivers, I/O drivers and receivers, fan motor.

The network is fed by the Host PC motherboard through the +3.3 V and the +12 V power rails of the PCI Express slot connector. Protection fuses inserted at the input side of each power rail prevent potential fire hazards.

The **board status LED lamp** reflects the global status of all the power converters of the main distribution network.

PCIe Products - Auxiliary power distribution network

The auxiliary power distribution network delivers power to the external devices including:

- CoaXPress cameras using the PoCXP capability available on all connections of the CoaXPress Host connector
- System devices using the +12 V power output available on all I/O connectors

The network is fed by a 12 V external power supply attached to the auxiliary power input connector using a power cable terminated by a 6-pin PEG plug connector. A protection fuse inserted at the input side prevents potential fire hazards.

A 24-volt DC power converter provides power to each camera connection through a PoCXP transmitter unit. Each PoCXP transmitter unit implements an electronic fuse/switch. A PTC inserted at the input of each transmitter unit prevents potential fire hazards.

The +12 V power is distributed from a common electronic fuse to all the I/O connectors. A PTC inserted at the input of prevents potential fire hazards.

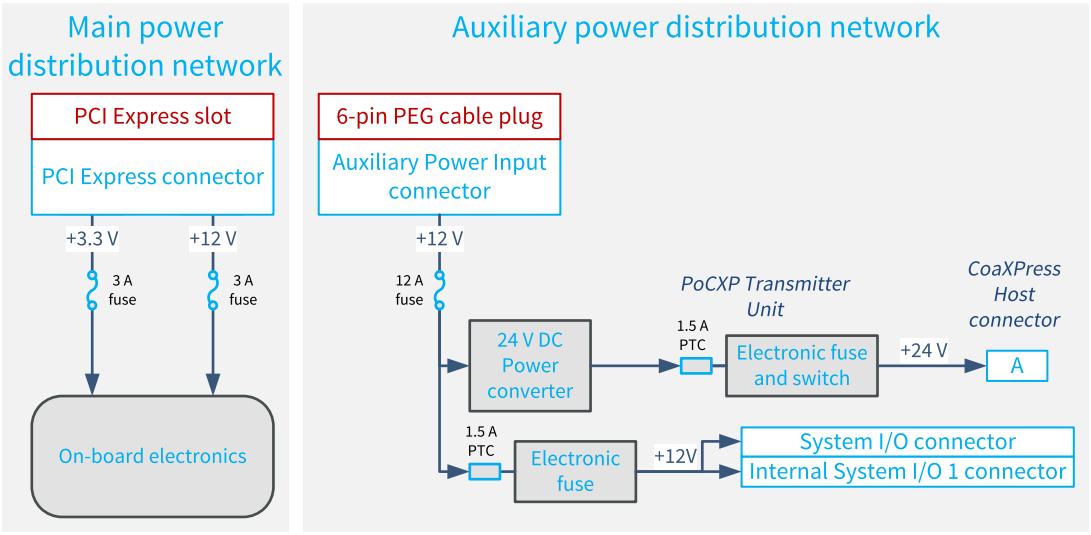
The "CoaXPress Lamps" on page 41 reflect the state of each CoaXPress host connection.

The following auxiliary power distribution network status are reported to the application:

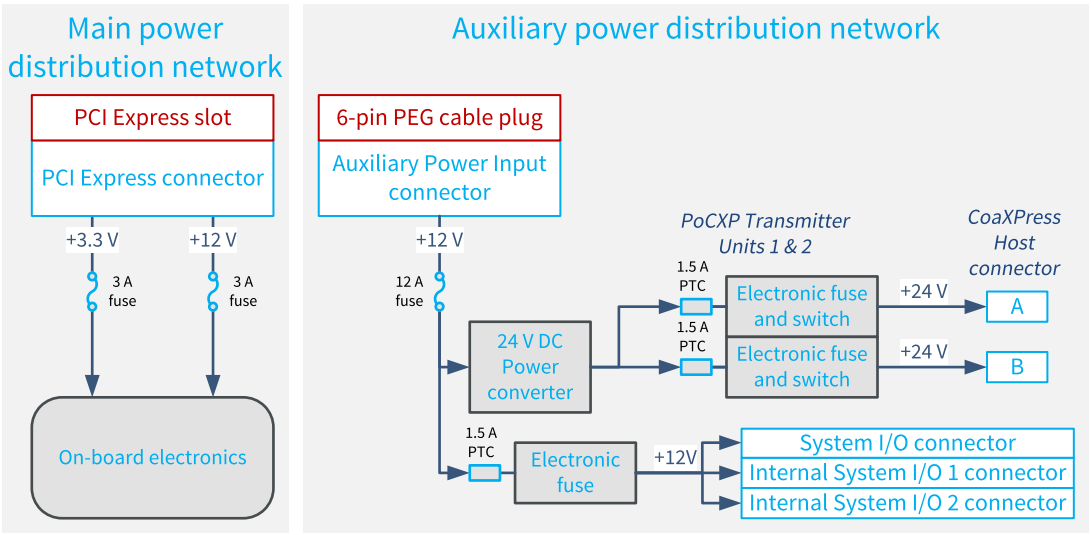
- Presence of a PEG cable and a PEG compliant power supply
- Valid 12 V voltage measured after the 12 A fuse.

- 24 V DC power converter status
- Output current and output voltage of each PoCXP transmitter

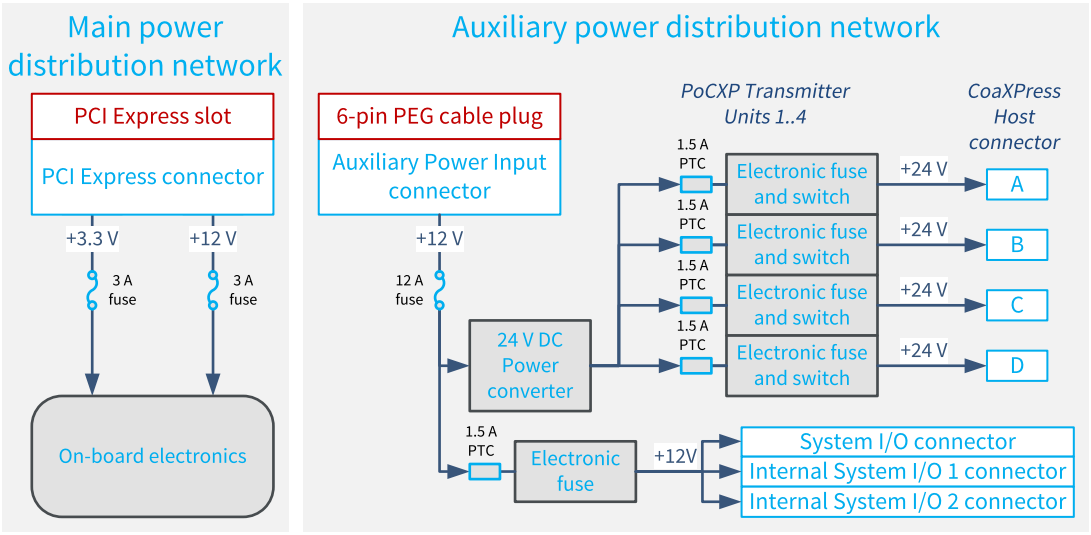
1630 Coaxlink Mono power distribution scheme



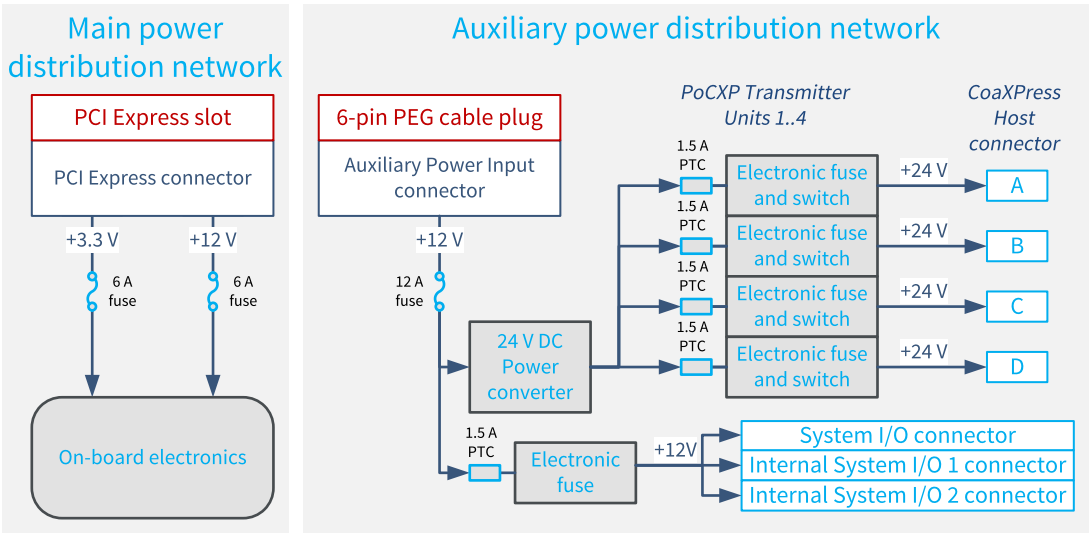
1631 Coaxlink Duo power distribution scheme



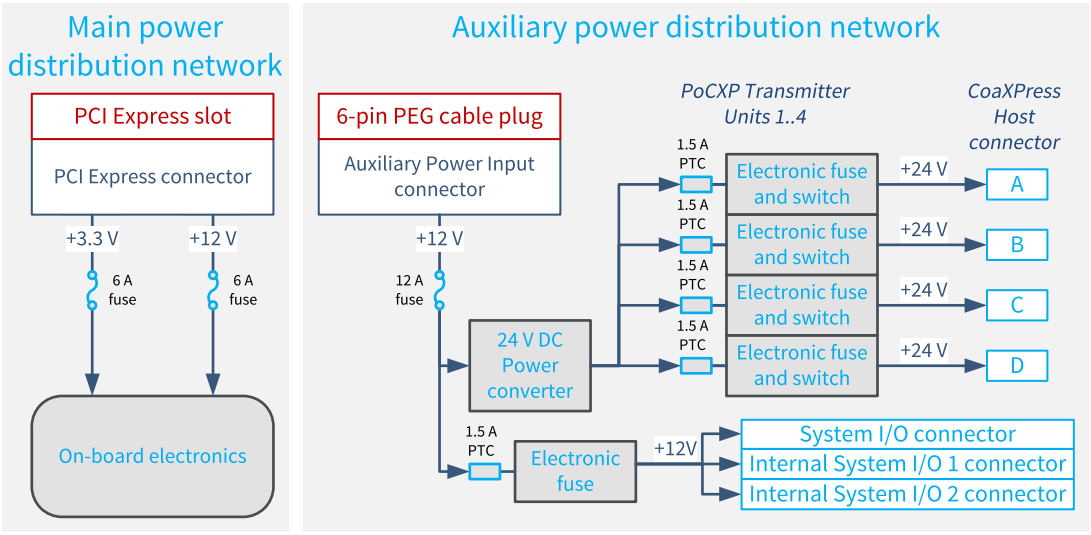
1632 Coaxlink Quad power distribution scheme



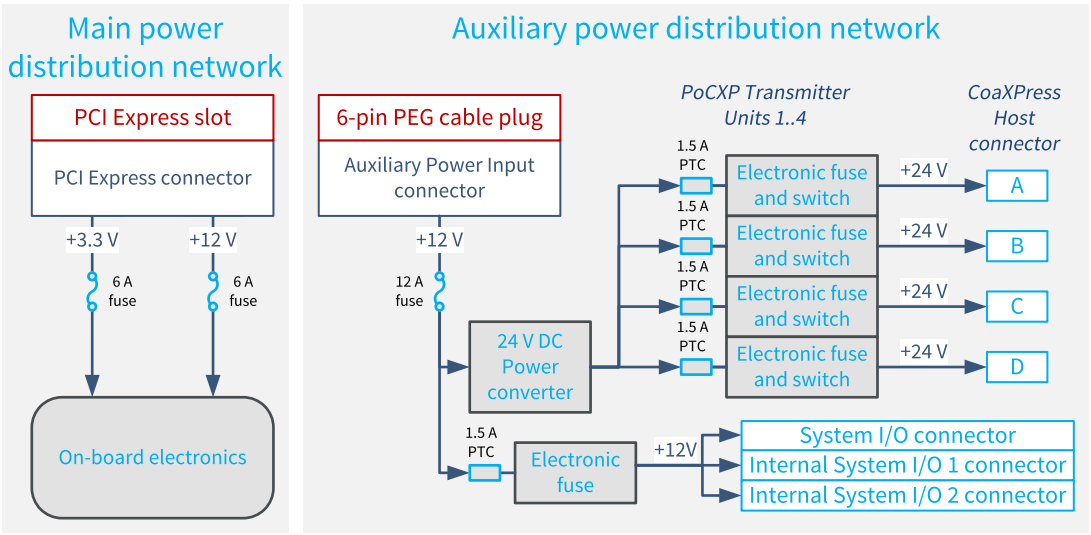
1633 Coaxlink Quad G3 power distribution scheme



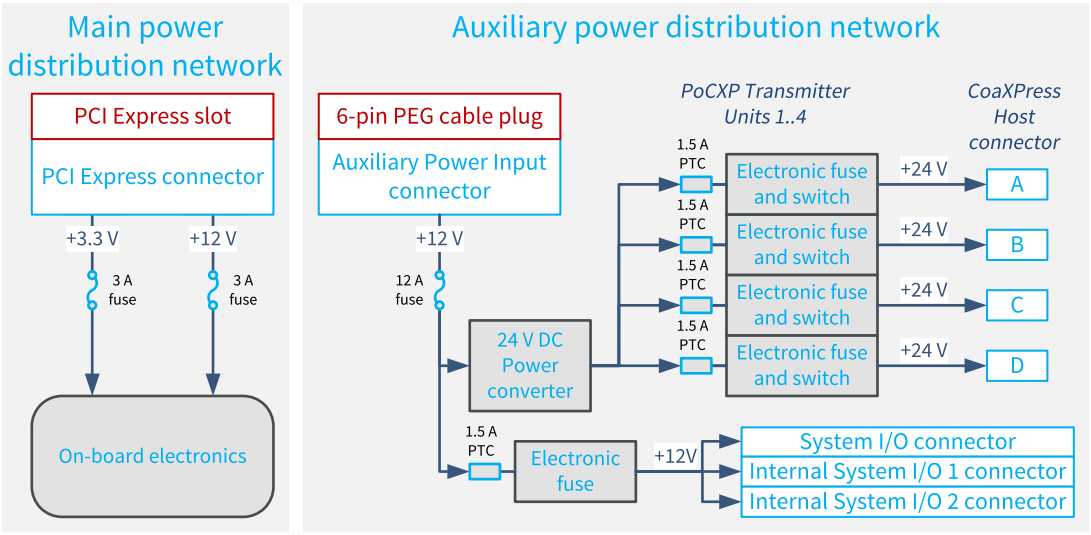
1635 Coaxlink Quad G3 DF power distribution scheme



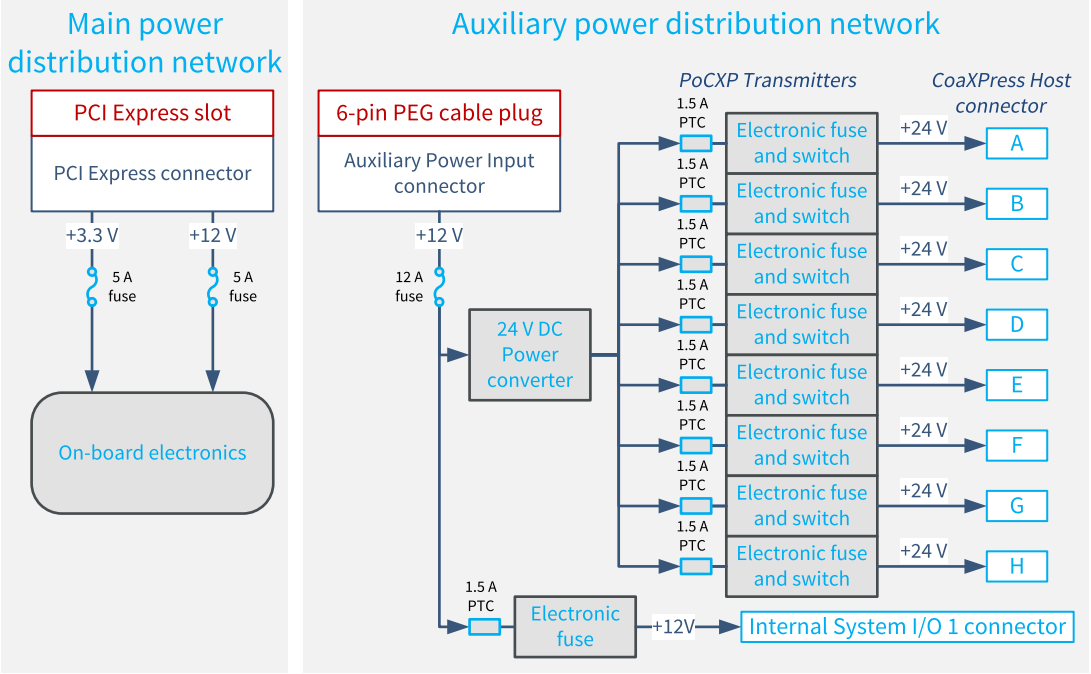
1637 Coaxlink Quad 3D-LLE power distribution scheme



1638 Coaxlink Quad CXP-3 power distribution scheme



3602 Coaxlink Octo power distribution scheme



Note: *The fuses are not serviceable! When blown, the card must be returned to the factory.*

Note: *PTCs and electronic fuses are self-resettable fuses.*

Note: *The Coaxlink card can be operated without applying power to the auxiliary power distribution network.*

3.4. PCI Express Power

PCI Express power requirements specification

1630 Coaxlink Mono

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V
+3.3 V power		2.1		W
+12 V power		7.2		W
Total power		9.3		W

1631 Coaxlink Duo

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V
+3.3 V power		2.7		W
+12 V power		8.7		W
Total power		11.4		W

1632 Coaxlink Quad

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V
+3.3 V power		2.5		W
+12 V power		9.6		W
Total power		12.1		W

1633 Coaxlink Quad G3

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V
+3.3 V power		3.8		W
+12 V power		13		W
Total power		16.8		W

1635 Coaxlink Quad G3 DF

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V
+3.3 V power		3.8		W
+12 V power		13		W
Total power		16.8		W

1637 Coaxlink Quad 3D-LLE

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V
+3.3 V power		3.8		W
+12 V power		13		W
Total power		16.8		W

1638 Coaxlink Quad CXP-3

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V
+3.3 V power		2.5		W
+12 V power		9.6		W
Total power		12.1		W

3602 Coaxlink Octo

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V
+3.3 V power		4.2		W
+12 V power		11.8		W
Total power		16.0		W

The typical power values were measured under the following conditions:

- Acquiring image data using all CoaXPress Host Interface connections operating at their maximum speed
- Delivering image data on the PCI Express configured for the largest link width and the highest link speed
- Operating @25°C [77 °F] ambient temperature and nominal supply voltages

3.5. Auxiliary Power

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo QuadCXP12

Specification of the auxiliary power input

1630 Coaxlink Mono

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12W I/O output power	0		12	W
DC input power for PoCXP	17W PoCXP output power			19	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

1631 Coaxlink Duo

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12W I/O output power	0		12	W
DC input power for PoCXP	34W total PoCXP output power			37	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

Quad CoaXPress Host Connector Products

Applies to: Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE QuadCXP12

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12W I/O output power	0		12	W
DC input power for PoCXP	68W total PoCXP output power			74	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

3602 Coaxlink Octo

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12W I/O output power	0		12	W
DC input power for PoCXP	136W total PoCXP output power			148	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

Note: *The sense input of the PEG connector is intended for power source cable presence detection. It should be grounded at the power supply level.*

Note: *The power rating of the power source is application dependent.*

3.6. I/O Power Output

Specification of the +12V power output of the I/O connector

A non-isolated +12 V power output is available on every I/O connector.

The power originates from an external 12 V power supply plugged into the Auxiliary Power Input connector. It is distributed from a common electronic fuse to all the I/O connectors.

The electronic fuse provides the following protections:

- Limits the inrush current during power on sequence
- Protects the Coaxlink card and the power source against overload
- Protects the Coaxlink card the power source against short-circuits.

The sum of the load currents drawn from all the 12 V outputs of the I/O connectors must be lower or equal to the specified maximum output current.

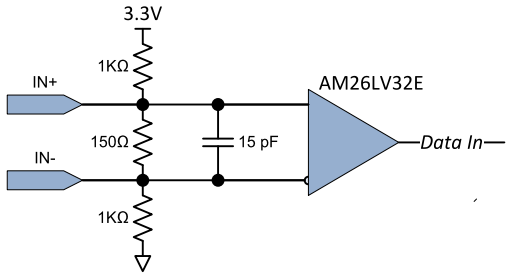
I/O +12 V power output specification

Parameter	Conditions	Min.	Typ.	Max.	Units
Aggregated output current	Operating temperature range			1.0	A
Voltage drop across the electronic fuse	Max. output current			0.2	V

Note: *The above specification applies over the whole operating temperature range of the Coaxlink card.*

3.7. Differential Input

Specification of the differential GPIO input ports



Differential Input Simplified Schematic

The receiver complies with the ANSI/TIA/EIA-422B specification.

DC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Common mode voltage		-7		+7	V
Differential sensitivity				200	mV
Input impedance			120		Ohm
ESD protection	Human Body Model (HBM)	15			kV
	Contact discharge	8			kV
	Air gap discharge	15			kV

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	100			ns
Pulse rate	0		5	MHz
10%-90% rise/fall time			1	µs

Logical map

The state of the port is reported as follows:

Differential Input voltage	Logical State
(VIN+ - VIN-) > +200 mV	HIGH
(VIN+ - VIN-) < - 200 mV	LOW
Unconnected input	HIGH

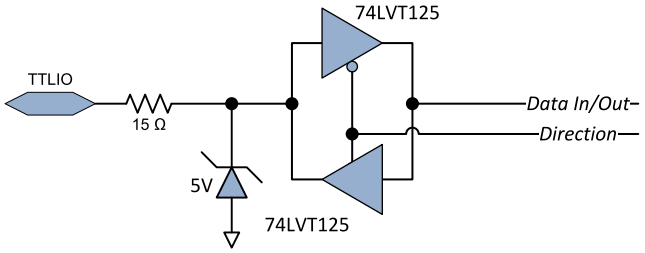
Compatible drivers and receivers

The following drivers are compatible with the high-speed differential input ports:

- ANSI/EIA/TIA-422/485 differential line drivers
- Complementary TTL drivers

3.8. TTL Input/Output

Specification of the TTL GPIO input/output ports



TTL Input/Output Simplified schematic

The receiver is LVTTL and 5 V TTL compliant. The driver is a 3.3 V TTL driver.

DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Common mode input voltage		0		5	V
Low-level output current				64	mA
Low-level output voltage	@ 8 mA		0.34	0.36	V
	@ 16 mA		0.48	0.55	V
	@ 32 mA		0.78	0.81	V
	@ 64 mA		1.34	1.36	V
High-level output current				-32	mA
High-level output voltage	@-8 mA; (1)	2.60	3.00		V
	@-16 mA; (1)	2.20	2.70		V
	@-32 mA; (1)	1.75	2.20		V
ESD protection	Human Body Model (HBM)	2			kV

Condition (1): 300 Ohms line termination resistor to GND.

Note: *The I/O port includes a latch-up protection.*

AC characteritics

Parameter	Conditions	Min.	Typ.	Max.	Units
Pulse width		100			ns
Pulse rate		0		5	MHz
10%-90% rise/fall time	(1)		10	20	ns

Condition (1): Short cable (1 m) and a 300 Ohms line termination resistor to GND.

Logical Map

The state of the port is reported as follows:

Input voltage	Logical State
VIN > 2.0 V	HIGH
VIN < 0.8 V	LOW
Unconnected input port	*Undetermined*

Compatible drivers and receivers

The following drivers are compatible:

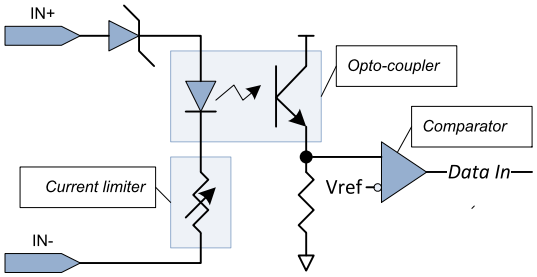
- Totem-pole LVTTL, TTL, 5 V CMOS drivers

The following receivers are compatible:

- LVTTL, TTL, 3-Volt CMOS receivers

3.9. Isolated Input

Specification of the isolated GPIO input ports

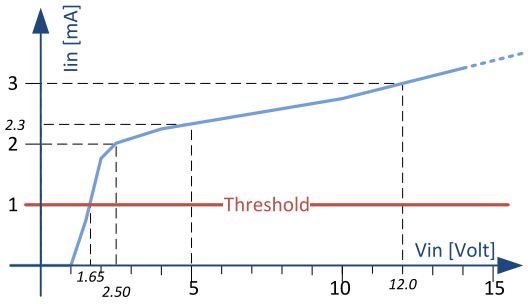


Isolated Input Simplified schematic

The input port implements an isolated current-sense input.

DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential voltage		-30		+30	V
Input current threshold			1		mA
Differential voltage	@1 mA	1.5	1.65	1.9	V
Input current	@(VIN+ - VIN-) = 1.65 V		1		mA
	@(VIN+ - VIN-) = 2.5 V		2		mA
	@(VIN+ - VIN-) = 5 V		2.3		mA
	@(VIN+ - VIN-) = 12 V		3		mA
	@(VIN+ - VIN-) = 30 V			5	mA
	@(VIN+ - VIN-) < 1 V			10	µA
DC isolation voltage		250			V
AC isolation voltage		170			V_{RMS}



Input Current vs. Input Voltage Characteristics

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	10			µs
Pulse rate	0		50	kHz

Logical map

The state of the port is reported as follows:

Input current	Logical State
IIN > 1 mA	HIGH
IIN < 1 mA	LOW
Unconnected input port	LOW

Compatible drivers and receivers

The following drivers are compatible with the isolated current-sense inputs:

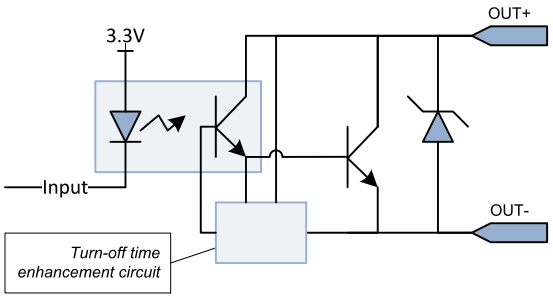
- Totem-pole LVTTL, TTL, 5 V CMOS drivers
- RS-422 Differential line drivers
- Potential free contact, solid-state relay, or opto-isolators
- 12 V and 24 V signaling voltages are also accepted

Note: *The +12 V power supply on the I/O connector(s) can be used for powering drivers requiring a power supply.*

Note: *No external resistors are required. However, to obtain the best noise immunity with 12 V and 24 V signaling, it is recommended to insert a series resistor in the circuit. The recommended resistor values are: 4.7k Ohms for 12 V signaling and 10k Ohms for 24 V signaling.*

3.10. Isolated Output

Specification of the isolated GPIO output ports



Isolated Output Simplified schematic

The output port implements an isolated contact output.

DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Current				100	mA
Differential voltage	Open state	-30		30	V
	Closed state @ 1 mA			0.4	V
	Closed state @ 100 mA			1.0	V
DC isolation voltage		250			V
AC isolation voltage		170			V_{RMS}

Note: *The output port in the closed state has no current limiter, the user circuit must be designed to avoid excessive currents that could destroy the output port.*

Note: *The output port remains in the OFF-state until it is under control of the application.*

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse rate	0		100	kHz
Turn-on time			5	µs
Turn-off time			5	µs

Typical switching performance @ 25°C

Current [mA]	Turn ON time [µs]	Turn OFF time [µs]
0.5	2.0	4.8
1.0	2.0	3.9
4.0	2.2	3.3
10	2.3	2.7
40	2.3	2.7
100	2.3	2.7

Logical map

The state of the output port is determined as follows:

Logical State	Output port state
HIGH	The contact switch is closed (ON)
LOW	The contact switch is open (OFF)

Compatible loads

The following loads are compatible with the isolated contact output ports:

- Any load within the 30V / 100 mA envelope is accepted. The power originates from an external power source or alternatively from the power delivered through the 12V and GND pins of the I/O connectors.

4. Environmental Specification

Environmental specification of the product(s) including: climatic requirements, electromagnetic standards compliance statements, safety standards compliance statements, etc.

4.1. Environmental Conditions

Storage and operating conditions specification of standard climatic class products

Storage Conditions

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo

Parameter	Conditions	Min	Max	Units
Ambient air temperature		-20 [-4]	70 [158]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

Operating Conditions

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo QuadCXP12

Parameter	Conditions	Min	Max	Units
FPGA die temperature			80 [176]	°C [°F]
Ambient air temperature		0 [32]	55 [131]	°C [°F]
Ambient air humidity	Non-condensing	0	100	% RH

Important: *The thermal design of the host PC must ensure that, at any time, the FPGA die temperature never exceeds the recommended limit.*

Warning: *Exceeding the upper limit of the FPGA die temperature can permanently damage the card.*

Note: *The Coaxlink cards are equipped with a temperature sensor that reports the temperature of the FPGA die.*

Note: *An event is reported to the application when the FPGA die temperature reaches the limit.*

4.2. Thermal Data

Heat sources and heat extraction method

PCI Express products

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo

The main heat contributors are:

The electronic devices of the Coaxlink card including the losses of the power converters of the **main** power distribution network.

The losses of the 24 V power converter of the **auxiliary** power distribution network. This contribution depends on the delivered PoCXP power.

Estimated heat power [W]

Product	Main	Auxiliary	Total
1630 Coaxlink Mono	9.3	0 ~ 1.3	9.3 ~ 10.6
1631 Coaxlink Duo	11.4	0 ~ 2.7	11.4 ~ 14.1
1632 Coaxlink Quad	12.1	0 ~ 5.5	12.1 ~ 17.6
1633 Coaxlink Quad G3	16.8	0 ~ 5.5	16.8 ~ 22.3
1635 Coaxlink Quad G3 DF	16.8	0 ~ 5.5	16.8 ~ 22.3
1637 Coaxlink Quad 3D-LLE	16.8	0 ~ 5.5	16.8 ~ 22.3
1638 Coaxlink Quad CXP-3	12.1	0 ~ 5.5	12.1 ~ 17.6
3602 Coaxlink Octo	16.0	0 ~ 11	16.0 ~ 27.0

Note: *The data of the auxiliary column are calculated with 17 W of PoCXP per connector and a worst case 24V DC/DC converter efficiency of 92.5%..*

The heat produced by the board is dissipated into the ambient air inside the Host PC. The heat exchange is facilitated by a heat sink and a fan mounted on the FPGA (the component having the largest heat source).

The thermal design must ensure sufficient air flow along both sides to keep the FPGA die temperature below the upper limit of the allowed temperature range. The application is responsible for regularly checking the temperature and for taking the appropriate action in case of excessive temperature.

4.3. Compliances

Compliance statements.

CE Compliance Statement

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo QuadCXP12

Notice for Europe

This product is in conformity with the Council Directive 2014/30/EU

This piece of equipment has been tested and found to comply with Class B EN55022/CISPR22 electromagnetic emission requirements and Class A EN55024/CISPR24 electromagnetic susceptibility.

This product has been tested in typical class A and class B compliant host systems. It is assumed that this product will also achieve compliance in any class A or class B compliant unit.

To meet EC requirements, shielded cables must be used to connect a peripheral to the card.

FCC Compliance Statement

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo QuadCXP12

Notice for USA

Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation or when the equipment is operated in a commercial environment.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

RoHS Compliance Statement

This product is in conformity with the European Union RoHS 2011/65/EU Directive, that stands for "the restriction of the use of certain hazardous substances in electrical and electronic equipment".

WEEE Statement

According the European directive 2012/19/EU, the product must be disposed of separately from normal household waste. It must be recycled according to the local regulations.

5. Related Products & Accessories

5.1. 1636 InterPC C2C-Link Adapter

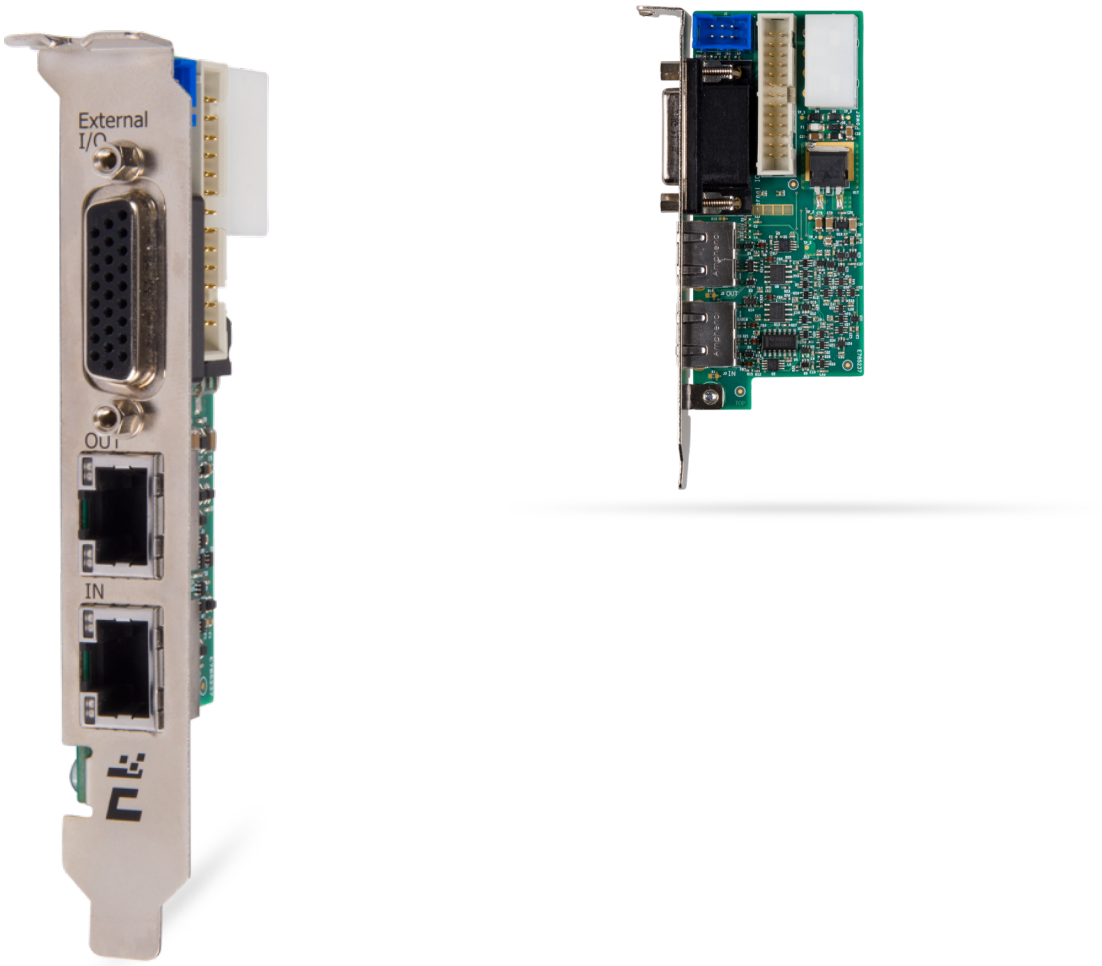
The 1636 InterPC C2C-Link Adapter is an accessory product for use as an **InterPC C2C-Link extender** and/or as a **HD26F I/O adapter.**

For a 1636 InterPC C2C-Link Adapter hardware description, refer to "Hardware Description" on page 82.

For a description of the C2C-Link extender usage, refer to "Using 1636 as C2C-Link Extender" on page 85.

For a description of the HD26F I/O adapter usage, refer to "Using 1636 as HD26F I/O Adapter" on page 84.

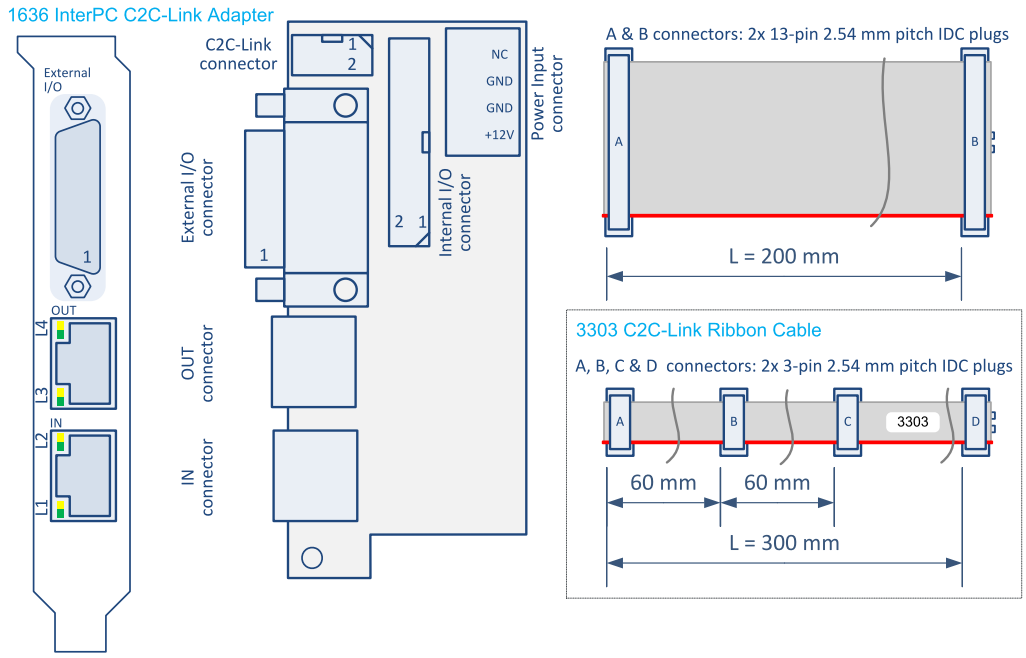
Product Pictures



Pictures of 1636 InterPC C2C-Link Adapter

Hardware Description

Layout



1636 InterPC C2C-Link Adapter

The 1636 InterPC C2C-Link Adapter product accessory is composed of:

- A printed circuit board assembly fitted with a standard-profile PC bracket.
- A 200-mm 26-way ribbon cable.
- A 3303 C2C-Link Ribbon Cable.

Connectors

The **External I/O connector** is a HD26F – 26-pin 3-row high-density female – Sub-D connector fitted on the bracket with UNC 4-40 screws. Refer to "Using 1636 as HD26F I/O Adapter" on page 84 for the usage description and the pin assignments.

The **IN connector** and the **OUT connector** are RJ-45 8-pin sockets fitted on the bracket. Refer to "Using 1636 as C2C-Link Extender" on page 85 for the usage description.

The **Internal I/O connector** is a 26-pin dual-row 0.1" pitch pin header with shrouding. Refer to "Using 1636 as HD26F I/O Adapter" on page 84 for the usage description and the pin assignments.

The **C2C-Link connector** is a 6-pin dual-row 0.1" pitch pin header with shrouding. Refer to "Using 1636 as C2C-Link Extender" on page 85 for the usage description.

The **Internal I/O connector** is a 26-pin dual-row 0.1" pitch pin header with shrouding. Refer to "Using 1636 as HD26F I/O Adapter" on the next page for the usage description.

The **Power Input connector** is a 0.2" pitch right-angled Disk Drive Power connector. Refer to "Using 1636 as C2C-Link Extender" on page 85 for the usage description.

Lamps

The **IN connector** and the **OUT connector** are each equipped with 2 green/yellow LED lamps named respectively **L1**, **L2**, **L3** and **L4**. Refer to "Using 1636 as C2C-Link Extender" on page 85 topic for the usage description.

5.2. Using 1636 as HD26F I/O Adapter

To use 1636 InterPC C2C-Link Adapter as an HD26F I/O adapter:

- Plug the A-connector of the supplied 200-mm 26-way ribbon cable to the **Internal I/O** connector of the 1636 InterPC C2C-Link Adapter
- Plug the B-connector to the **Internal I/O** connector of the target card.

  Note: *No power supply connection is required when using the 1636 InterPC C2C-Link Adapter as an HD26F I/O adapter only.*

5.3. Using 1636 as C2C-Link Extender

Adapter Powering

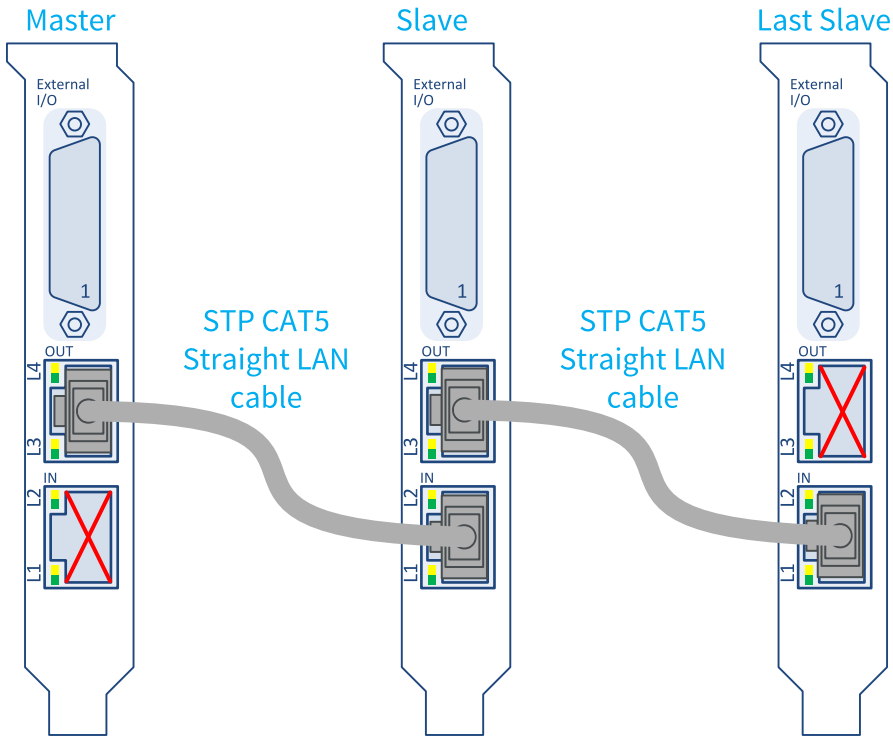
Important: *The 1636 InterPC C2C-Link Adapter must be powered when it is used as a C2C-Link extender.*

The user has two options to supply power to the adapter:

- From the Coaxlink card +12V power output through the 26-way ribbon cable attached to the **Internal I/O** connector.
- From the Host PC power supply through a Disk Drive Power connector cable plugged into the **Power Input connector**.

Parameter	Min.	Typ.	Max.	Units
+12 V DC Input voltage	11.0	12.0	13.0	V
+12 V Input power		1.8		W

InterPC Interconnect



External wiring of a C2C-Link across 3 adapters.

The external wiring of the C2C-Link is made with RJ 45 CAT 5 STP straight LAN cables. N-1 cables are required to interconnect N adapters in a daisy-chain scheme.

The daisy-chain begins on the OUT connector of the Master adapter and ends at the IN connector of the Last Slave adapter.

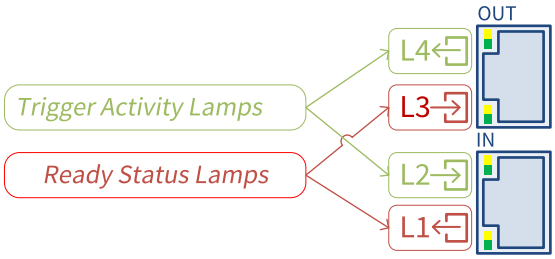
The IN connector of the Master adapter and the OUT connector of the Last Slave adapter are unused.

> **Note:** *The adapter disables the signal drivers of the IN and OUT connectors to avoid electrical damages when it detects a bad or a missing connection.*

The InterPC cable drivers and receivers are not electrically isolated.

> **Important:** *To avoid damages, the interconnected PCs must have a common ground reference.*

Lamps



1636 InterPC C2C-Link Adapter lamps

Trigger Activity Lamps

The L2 and L4 Lamps indicate the trigger activity on the LAN cable. L2 shows the activity on the received trigger signals; L4 shows the activity on the transmitted trigger signals.

Lamp State	Indication
Off	The LAN cable is unplugged or the adapter is not powered.
Green	No trigger activity. *No trigger events in the past 10 milliseconds.*
Yellow	Trigger activity. *One or more trigger events in the past 10 milliseconds.*

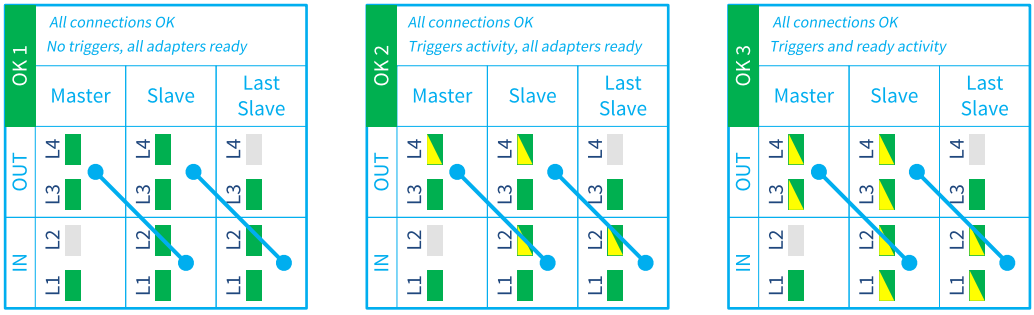
Ready Status Lamps

The L1 and L3 Lamps indicate the state of the ready signal on the LAN cable. L1 shows the state of the transmitted ready signal; L3 shows the state of the received ready signal.

Lamp State	Indication
Off	The adapter is not powered.
Green	Ready true. *For L1: all the C2C-Link devices attached to this adapter and the downwards adapters (if any) are ready.* *For L3: all the C2C-Link devices attached to the downwards adapters (if any) are ready.*
Yellow	Ready false. *For L1: one or more C2C-Link devices attached to this adapter and the downwards adapters (if any) are not ready.* *For L3: one or more C2C-Link devices attached to the downwards adapters (if any) are not ready.*

Note: *Unlike the trigger activity lamps, the ready signals are not enlarged. Short-duration not-ready states are hardly visible!*

Adapters Array Lamp States – Normal Situations



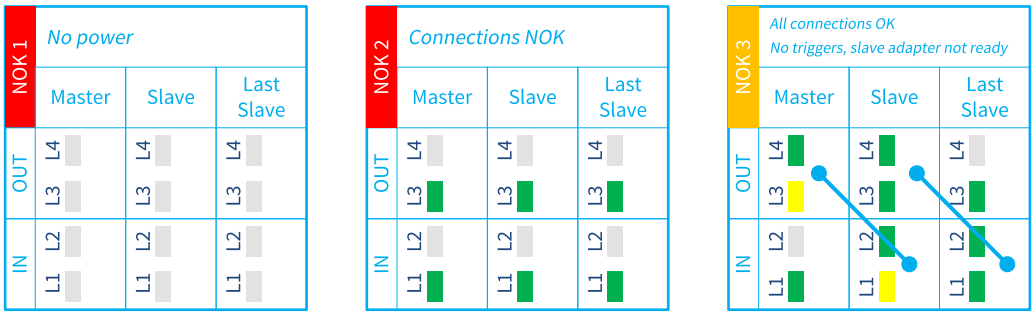
The above drawings show the lamps states of 3 daisy-chained adapters for 3 normal situations.

In the OK 1 situation, all adapters are ready to accept triggers but no triggers are sent by the master.

In the OK 2 situation, the master adapter sends triggers and the ready signal of all adapters is permanently high. The yellow/green toggling L2 and L4 lamps indicate the trigger activity. The steady green L1 and L3 lamps indicate that all adapters are permanently ready to receive triggers.

In the OK 3 situation, the master adapter sends triggers and the ready signal of all adapters is cycling. The yellow/green toggling L2 and L4 lamps indicate the trigger activity. The yellow/green toggling L1 and L3 lamps indicate that all adapters are not ready to receive triggers for a significant duration.

Adapters Array Lamp States – Abnormal Situations



The above drawings show the lamps states of 3 daisy-chained adapters for 3 abnormal situations.

In the NOK 1 situation, no adapters are powered. All lamps are Off.

In the NOK 2 situation, all adapters are powered but all connections are missing or incorrect.

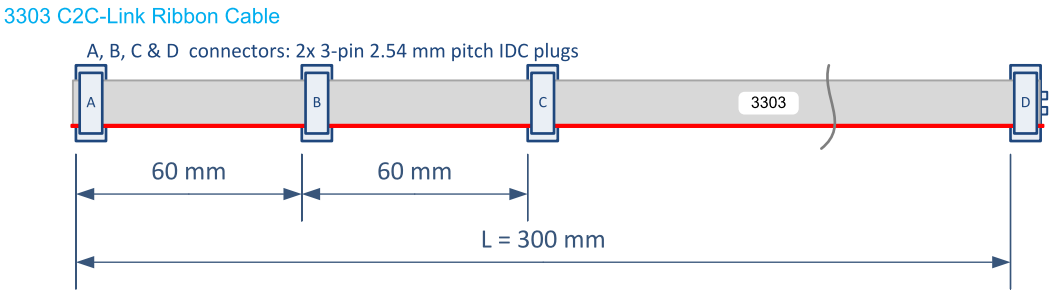
In the NOK 3 situation, all adapters are powered and all connections are OK, but the second adapter is not ready preventing the master to send new triggers. This situation is considered as abnormal when it persists.

Troubleshooting Guide

Lamps state	Indication and possible causes	Action
All lamps Off	The adapter is not powered.	Apply power to the adapter
L2 Off L1 Green	The external connection to the IN connector is missing or incorrect.	For the master adapter, this is OK: nothing to do! For the other adapters: check and correct the connection to the OUT connector of the previous adapter in the daisy-chain.
L4 Off L3 Green	The external connection to the OUT connector is missing or incorrect.	For the last slave adapter of the daisy-chain, this is OK: nothing to do! For the other adapters: check and correct the connection to the IN connector of the next adapter in the daisy-chain.

5.4. 3303 C2C-Link Ribbon Cable

3303 C2C-Link Ribbon Cable is an accessory product used for Intra-PC C2C-Link interconnection.



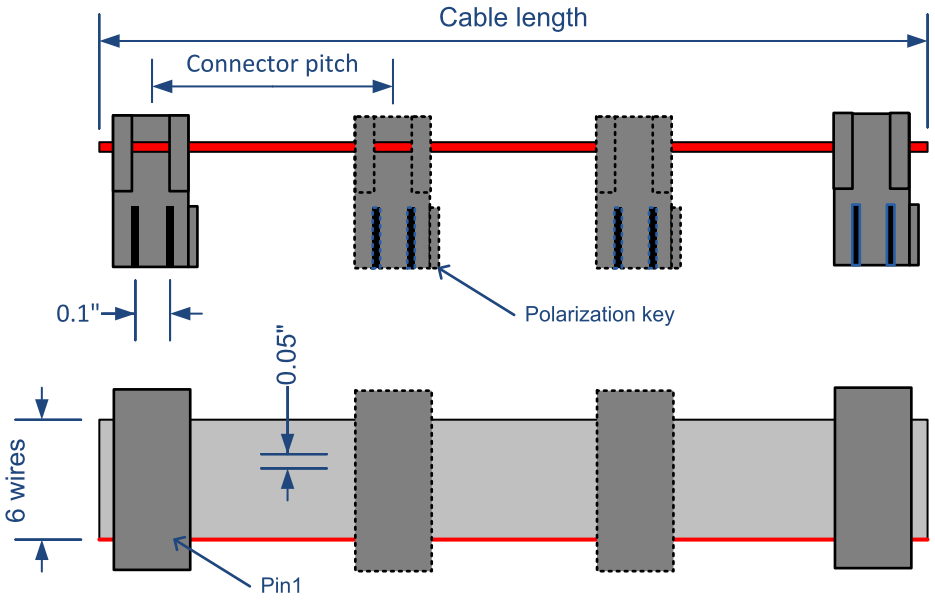
3303 C2C-Link Ribbon Cable assembly

The 3303 C2C-Link Ribbon Cable is a 6-conductor 0.05-in pitch ribbon fitted with 4 6-pin female ribbon cable connectors.

This cable is used for interconnecting the C2C-Link connectors of up to 4 cards located in the same PC.

5.5. Custom C2C-Link Ribbon Cable Assembly

Assembly instructions of a custom-made IntraPC C2C-Link interconnection.



Custom C2C-Link Ribbon Cable Assembly

The cable assembly is composed with:

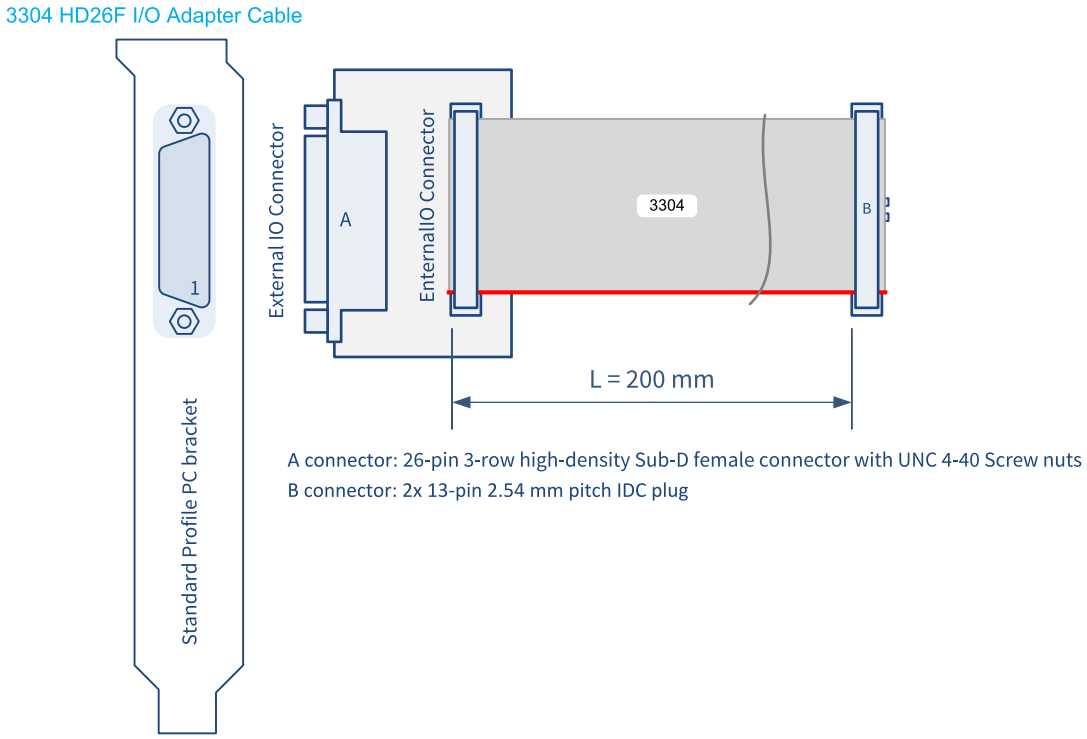
- A piece of a 6-conductor 0.05-in pitch ribbon cable. For instance: *Belden's (9L280XX Series)*.
- Two or more pieces of a 2 x 3-pin female ribbon cable connectors. For instance: *TE connectivity 1-1658528-1*.

The cable assembly has:

- A maximum of 4 connectors allowing up to 4 cards to share the same C2C-Link.
- A maximum length of 60 cm.

  Note: *The connector pitch(es) must be determined according to the actual card to card spacing in the Host PC.*

5.6. 3304 HD26F I/O Adapter Cable



The 3304 HD26F I/O Adapter Cable interconnects a 26-pin dual-row 0.1" pitch connector to a 26-pin 3-row female High-density SubD connector fitted into a standard-profile PC bracket.

Usage with Internal IO2 connector

Applies to: Duo Quad QuadG3 QuadCXP3 Quad3DLLE

The adapter brings the second set of I/O lines and the +12V power output to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1	1	GND	Ground
2	2	10	GND	Ground
3	3	20	DIN21+	High-speed differential input #21 – Positive pole
4	4	19	DIN21-	High-speed differential input #21 – Negative pole
5	5	13	DIN22+	High-speed differential input #22 – Positive pole
6	6	11	DIN22-	High-speed differential input #22 – Negative pole
7	7	3	IIN21+	Isolated input #21 – Positive pole
8	8	12	IIN21-	Isolated input #21 – Negative pole
9	9	13	IIN22+	Isolated input #22 – Positive pole
10	10	21	IIN22-	Isolated input #22 – Negative pole
11	11	14	IIN23+	Isolated input #23 – Positive pole
12	12	4	IIN23-	Isolated input #23 – Negative pole
13	13	15	IIN24+	Isolated input #24 – Positive pole
14	14	5	IIN24-	Isolated input #24 – Negative pole
15	15	23	IOUT21+	Isolated contact output #21 – Positive pole
16	16	22	IOUT21-	Isolated contact output #21 – Negative pole
17	17	16	IOUT22+	Isolated contact output #22 – Positive pole
18	18	6	IOUT22-	Isolated contact output #22 – Negative pole
19	19	25	TTLIO21	TTL input/output #21
20	20	24	GND	Ground (TTLIO21 return)
21	21	17	TTLIO22	TTL input/output #22
22	22	7	GND	Ground (TTLIO22 return)
23	23	8	-	Reserved
24	24	9	GND	Ground
25	25	26	+12V	+12 V Power output
26	26	18	GND	Ground (+12V return)

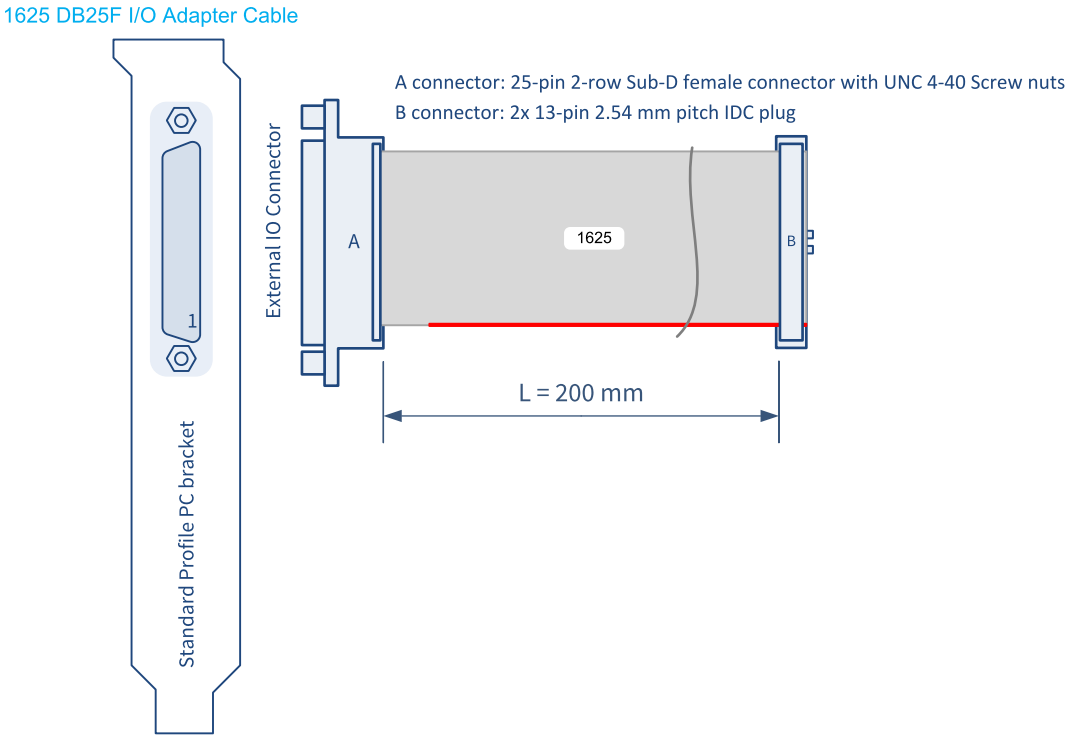
Usage with Internal IO1 connector

Applies to: QuadG3DF Octo

The adapter brings the second set of I/O lines and the +12V power output to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1	1	GND	Ground
2	2	10	GND	Ground
3	3	20	DIN11+	High-speed differential input #11 – Positive pole
4	4	19	DIN11-	High-speed differential input #11 – Negative pole
5	5	13	DIN12+	High-speed differential input #12 – Positive pole
6	6	11	DIN12-	High-speed differential input #12 – Negative pole
7	7	3	IIN11+	Isolated input #11 – Positive pole
8	8	12	IIN11-	Isolated input #11 – Negative pole
9	9	13	IIN12+	Isolated input #12 – Positive pole
10	10	21	IIN12-	Isolated input #12 – Negative pole
11	11	14	IIN13+	Isolated input #13 – Positive pole
12	12	4	IIN13-	Isolated input #13 – Negative pole
13	13	15	IIN14+	Isolated input #14 – Positive pole
14	14	5	IIN14-	Isolated input #14 – Negative pole
15	15	23	IOUT11+	Isolated contact output #11 – Positive pole
16	16	22	IOUT11-	Isolated contact output #11 – Negative pole
17	17	16	IOUT12+	Isolated contact output #12 – Positive pole
18	18	6	IOUT12-	Isolated contact output #12 – Negative pole
19	19	25	TTLIO11	TTL input/output #11
20	20	24	GND	Ground (TTLIO11 return)
21	21	17	TTLIO12	TTL input/output #12
22	22	7	GND	Ground (TTLIO12 return)
23	23	8	-	Reserved
24	24	9	GND	Ground
25	25	26	+12V	+12 V Power output
26	26	18	GND	Ground (+12V return)

5.7. 1625 DB25F I/O Adapter Cable



1625 DB25F I/O Adapter Cable

The 1625 DB25F I/O Adapter Cable connects all the pins (but the pin 1) of a 26-pin dual-row 0.1" pitch connector to a 25-pin female SubD connector fitted into a standard-profile PC bracket.

Usage with Internal IO2 connector

Applies to: Duo Quad QuadG3 QuadCXP3 Quad3DLLE

The adapter brings the second set of I/O lines and the +12V power output to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1		GND	Ground
2	2	1	GND	Ground
3	3	14	DIN21+	High-speed differential input #21 – Positive pole
4	4	2	DIN21-	High-speed differential input #21 – Negative pole
5	5	15	DIN22+	High-speed differential input #22 – Positive pole
6	6	3	DIN22-	High-speed differential input #22 – Negative pole
7	7	16	IIN21+	Isolated input #21 – Positive pole
8	8	4	IIN21-	Isolated input #21 – Negative pole
9	9	17	IIN22+	Isolated input #22 – Positive pole
10	10	5	IIN22-	Isolated input #22 – Negative pole
11	11	18	IIN23+	Isolated input #23 – Positive pole
12	12	6	IIN23-	Isolated input #23 – Negative pole
13	13	19	IIN24+	Isolated input #24 – Positive pole
14	14	7	IIN24-	Isolated input #24 – Negative pole
15	15	20	IOUT21+	Isolated contact output #21 – Positive pole
16	16	8	IOUT21-	Isolated contact output #21 – Negative pole
17	17	21	IOUT22+	Isolated contact output #22 – Positive pole
18	18	9	IOUT22-	Isolated contact output #22 – Negative pole
19	19	22	TTLIO21	TTL input/output #21
20	20	10	GND	Ground (TTLIO21 return)
21	21	23	TTLIO22	TTL input/output #22
22	22	11	GND	Ground (TTLIO22 return)
23	23	24	-	Not used
24	24	12	GND	Ground

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
25	25	25	+12V	+12 V Power output
26	26	13	GND	Ground (+12V return)

Usage with Internal IO1 connector

Applies to: QuadG3DF

The adapter brings the second set of I/O lines and the +12V power output to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1		GND	Ground
2	2	1	GND	Ground
3	3	14	DIN11+	High-speed differential input #11 – Positive pole
4	4	2	DIN11-	High-speed differential input #11 – Negative pole
5	5	15	DIN12+	High-speed differential input #12 – Positive pole
6	6	3	DIN12-	High-speed differential input #12 – Negative pole
7	7	16	IIN11+	Isolated input #11 – Positive pole
8	8	4	IIN11-	Isolated input #11 – Negative pole
9	9	17	IIN12+	Isolated input #12 – Positive pole
10	10	5	IIN12-	Isolated input #12 – Negative pole
11	11	18	IIN13+	Isolated input #13 – Positive pole
12	12	6	IIN13-	Isolated input #13 – Negative pole
13	13	19	IIN14+	Isolated input #14 – Positive pole
14	14	7	IIN14-	Isolated input #14 – Negative pole
15	15	20	IOUT11+	Isolated contact output #11 – Positive pole
16	16	8	IOUT11-	Isolated contact output #11 – Negative pole
17	17	21	IOUT12+	Isolated contact output #12 – Positive pole
18	18	9	IOUT12-	Isolated contact output #12 – Negative pole
19	19	22	TTLIO11	TTL input/output #11
20	20	10	GND	Ground (TTLIO11 return)
21	21	23	TTLIO12	TTL input/output #12

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
22	22	11	GND	Ground (TTLIO12 return)
23	23	24	-	Not used
24	24	12	GND	Ground
25	25	25	+12V	+12 V Power output
26	26	13	GND	Ground (+12V return)