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APPLICATION NOTES

Coaxlink

Coaxlink 10.3.1

PCI EXPRESS™

CoaXPress

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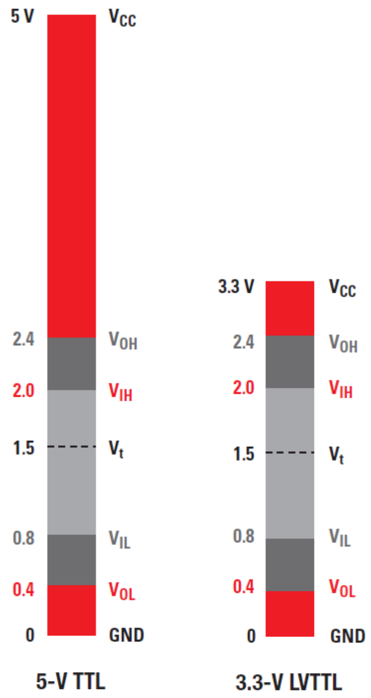
Contents

1. Connecting TTL Devices to Isolated I/O Ports

This application note explains how to connect TTL devices to the isolated inputs and isolated outputs.

1.1. TTL And LVTTL Voltage Levels



The figure above shows the respective voltage levels of a TTLand a LVTTL signaling interfaces using colored bars.

Driver Output

At the **low logic level**, the driver guarantees an output voltage within the *bottom red window*.

- The maximum driver output voltage, namely V_{OL} is 0.4 V for both TTL and LVTTL.
- The minimum driver output voltage is GND

At the **high logic level**, the driver output voltage is within the *upper red window*.

- The minimum driver output voltage, namely V_{OH} is 2.4 V for both TTL and LVTTL.
- The maximum driver output voltage is VCC: 5 V for TTL and 3.3 V for LVTTL

Receiver Input

The receiver guarantees to see a **low logic level** when the input signal voltage is within the *bottom red and dark gray windows*.

- The maximum receiver input voltage, namely V_{IL} is 0.8 V for both TTL and LVTTL.
- The minimum receiver input voltage is GND

The receiver guarantees to see a **high logic level** when the input signal voltage is within the *upper red and dark gray windows*.

- The minimum receiver input voltage, namely V_{IH} is 2.0 V for both TTL and LVTTL.
- The maximum receiver input voltage is VCC: 5 V for TTL and 3.3 V for LVTTL

  Note: *The dark gray window is a 0.4V noise margin between the driver output and the receiver input.*

  Important: *The light gray window is an area where the receiver cannot guarantee the logic level.*

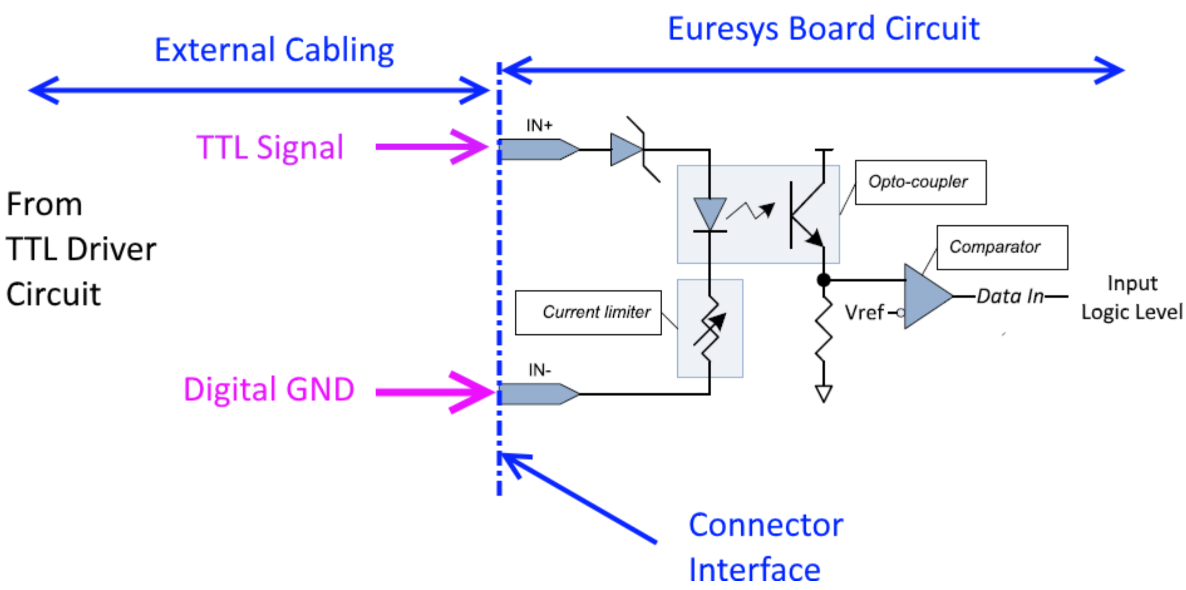
Typically the actual transition V_t between logic level low and high will occur at around 1.5V but the actual $V_t$level may change a lot according to specimens or process (P) variations , actual Vcc supply voltage (V), and temperature (T). Only V_{IL} and V_{IH} are guaranteed over P,V,T variations.

1.2. Connecting TTL Devices to Isolated Input Ports

Interfacing a device with a TTL or LVTTL output driver using a Coaxlink isolated input port

The isolated input ports of Coaxlink and Grablink products are, by design, compatible with TTL and LVTTL levels. No additional adapter is required to interconnect a (LV)TTL driver and an isolated input. The following section describes in detail how to connect them, what are the static voltage margins and what are the dynamic limitations.

Wiring Diagram



Connecting an (LV)TTL driver to an isolated input

Refer to Connectors for pin assignments.

1. Connect TTL Signal to IN+
2. Connect TTL Circuit Ground (Digital GND) to IN-

Important: *As good practice, it is recommended to shield the whole set of wires, using a shielded cable.Shielding improve EMI protection against external interferences (immunity) and avoid unwanted EM emissions. The shield should be connected to the devices (PC, cameras, and systems components) chassis and should be separated from the digital GND line.*

Static Levels Compatibility

(LV)TTL Driver Logic Level	(LV)TTL Driver Voltage Level	Isolated-Input Voltage Level	Voltage Margin	Isolated Input Logic Level
Low	0.4V max	1.5V max	1.1V	Low
High	2.4V min	1.9V min	0.5V	High

The above table shows that the voltage levels are well compatible and that they remains acceptable voltage margins for both TTL and LVTTL applications.

Refer to "Isolated Input" on page 24 for electrical specifications of isolated inputs.

Note: *Note the circuit does not perform logic level inversion.*

Note: *The isolated input needs about 1 mA of current at high logic level. This is compatible with the current drive capabilities of (LV)TTL drivers at , as most (LV)TTL drivers provides +/-16 mA. Even old TTL technologies provides 4 mA min in any case.*

Dynamic Limitations

Isolated inputs requires a minimum pulse high of 10 µs. The highest achievable pulse rate is 50 KHz.

Isolated inputs adds an extra delay of typically 5 µs (10 µs maximum).

Note: *The delay can be sometimes ignored and sometimes not, according to the application. For probably all the area-scan applications, such delay can be ignored, as is it very short compared to the camera cycle. For instance, such delay represents only 0.5 % of the cycle time of a super-fast 1,000 fps camera.For line-scan applications, the delay becomes significant since the camera cycle rate is much higher.*

1.3. Connecting TTL Devices to Isolated Output Ports

Interfacing a device with a TTL or LVTTL receiver using a Caoxlink isolated output port

Power must be provided to the opto-coupler transistor in order to operate the circuit.

Two cases are considered:

1. Refer to "Using External Power " below when an external 5V or 3.3V power supply line is available and can be carried to the opto-coupler(s) V_{out}+ pin(s).
2. Refer to "Using Local 12 V Power" on page 11 when the power is taken from the board itself, namely through the +12V power line connector pin.

Using External Power

The power supply voltage is not taken from the board but comes from the “external” system. A 3.3V or also 5V power supply can be considered, as most LVTTL input receiver circuits support 5V levels at their inputs. The power supply line must be carried through the cable up to the OUT+ pin of the opto-coupler.

In this case the voltage rail is called V_{CC}, as the voltage could be the same as the TTL receiver V_{CC} pin.

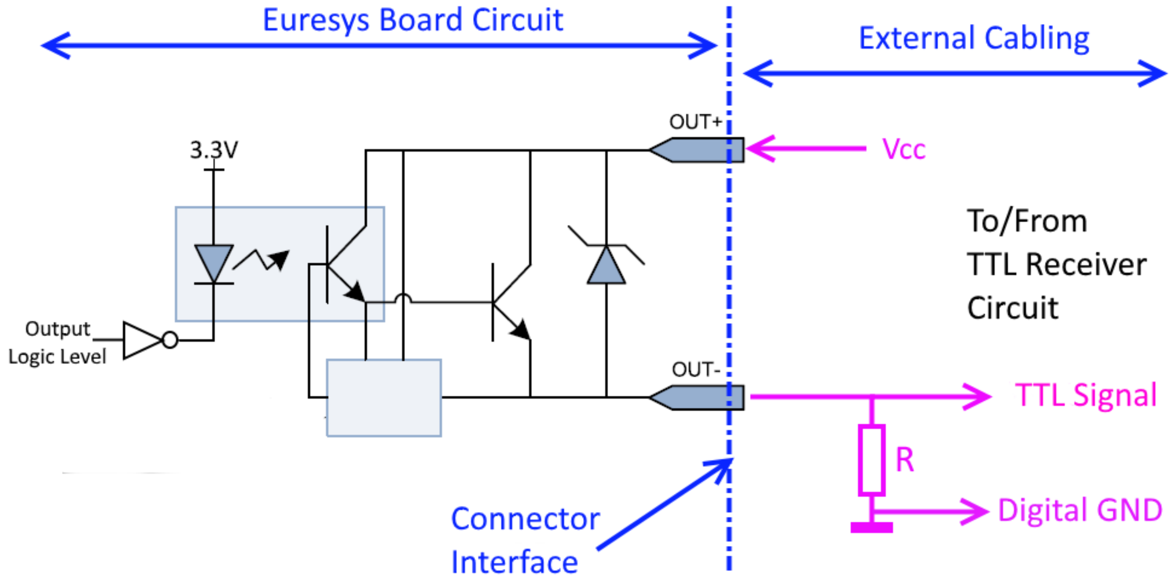
This circuit needs only one pull-down resistor as show in the next figure. A resistor of 180 ohm 1/8W is suggested as best compromise but the circuit can also work within a large range of resistor values from 50 ohm 1/2W to 10K ohm 1/16 W (1).

If an existing pull-down resistor is already available at the TTL receiver side it can be used as R resistor to operate the circuit, avoiding the need of adding an extra resistor somewhere in the cabling.

The circuit does not perform logic level inversion.

Note: *The resistor value can be also changed to match special "Static Levels Compatibility " on the next pageor "Dynamic Limitations " on page 11performance requirements. This topic is covered in the coming paragraphs.*

Wiring Diagram



Connecting an isolated output to a TTL receiver using the receiver's V_{CC} supply

Refer to Connectors for I/O connectors pin assignments.

1. Connect OUT+ to TTL V_{CC}. Nominally, V_{CC} should be 3.3V or 5V.
2. Connect OUT- to the TTL input.
3. Pull-down OUT- with a resistor (R) of 180 ohm 1/8W (or another resistor value that suits the circuit requirements).

   Important: *As good practice, it is recommended to shield the whole set of wires, using a shielded cable. Shielding improve EMI protection against external interferences (immunity) and avoid unwanted EM emissions. The shield should be connected to the devices (PC, cameras, and systems components) chassis and should be separated from the digital GND line.*

Static Levels Compatibility

The following tables show that the voltage levels are well compatible and that they remains acceptable voltage margins for both TTL and LVTTL applications.

Voltage levels and margins in a TTL (5V) system, R = 180 ohm

Isolated Output Logic Level	Isolated Output State	Isolated Output Voltage Level	TTL Input Voltage Level	Voltage Margin	TTL Input Logic Level
High	Close	4.1 V max (2)	2.0 V min	2.1 V	High
Low	Open	0.36 V max (1)	0.8 V max	0.44 V	Low

Voltage levels and margins in a LVTTL (3.3V) system, R = 180 ohm

Isolated Output Logic Level	Isolated Output State	Isolated Output Voltage Level	TTL Input Voltage Level	Voltage Margin	TTL Input Logic Level
High	Close	2.4 V min(2)	2.0 V min	0.4 V	High
Low	Open	0.36 V max(1)	0.8 V max	0.44 V	Low

Refer to "Isolated Output" on page 26 for voltage levels of isolated outputs.

Note 1 0.36V is obtained considering a worst-case external (pull-up) load of 2 mA (180 ohm x 2 mA = 0.36V), which means that the circuit can support the presence of an external pull-up resistor up to a (minimum) value of 1K5 ohm (in 3.3V) or 2K4 ohm (in 5V). If needed, an other R value can be chosen according to the actual pull-up load within the circuit.

Note 2 In any case, the voltage drop across the opto-coupler pins (V_{OUT}^+ - $V_{OUT}t^-$) is lower than 0.9V. Which gives the following results: 3.3V – 0.9V = 2.4V; 5V – 0.9V = 4.1V.

Dynamic Limitations

The maximum pulse width of isolated outputs is about 5 µs and the maximum pulse rate is 100 KHz,

Isolated outputs add an extra delay of about 5 µs in the signal propagation.

The resistor value of R = 180 ohm has good dynamic results for a usual capacitive loads as 1 or 2 meters of cable. As example, a 2m cable will add 100 pF of load (50pF/m) which give a rise time of about 18 µs at 180 ohm (R x C = 180 ohm x 100 pF = 18 µs) . If needed, the R value can be adapted to match special requirements in terms of rise time and/or capacitive load.

If maximizing the opto-coupler switching time is a concern, it is not recommended to not increase too much the value of the resistor. The opto-coupler circuit behaves better (switching times) with a load of about 10 mA or higher. R = 180 ohm loads the opto-coupler at 13 mA (3.3V) and 23 mA (5V).

Using Local 12 V Power

The power supply voltage is taken from the I/O connector itself, using the power supply pin “+12V”.

This circuit needs two resistors, named R and R_{POL}.

A resistor of 180 ohm 1/8W is suggested for R, as best compromise but the circuit can also work within a large range of resistor values from 50 ohm 1/2W to 10K ohm 1/16 W (1).

A resistor of 560 ohm 1/4W is suggested for R_{POL}, as best companion of R = 180 ohm but the value of R_{POL}can be adapted to match accordingly others R values.

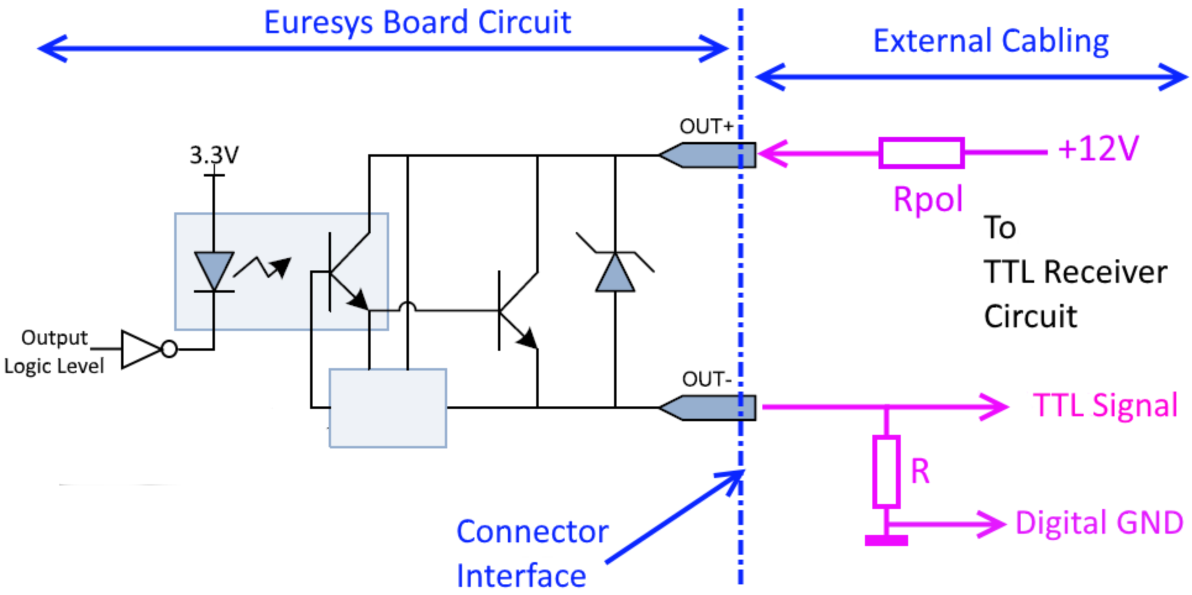
If an existing pull-down resistor is already available at the TTL receiver side it can be used as R resistor to operate the circuit, avoiding the need of adding an extra resistor somewhere in the cabling.

The circuit does not perform logic level inversion.

Note: *The resistor value can be also changed to match special static or dynamic performance requirements.*

Note: *The circuit does not perform logic level inversion.*

Wiring Diagram



Refer to Connectors for I/O connectors pin assignments.

1. Connect OUT+ to +12V through a resistor (R_{POL}) of 560 ohm 1/4 W (or another resistor value that suits the circuit requirements).
2. Connect OUT- to the TTL input.
3. Pull-down OUT- with a resistor (R) of 180 ohm 1/8W (or another resistor value that suits the circuit requirements).

Static Levels Compatibility

The following table shows that the voltage levels are well compatible and that they remains acceptable voltage margins for both TTL and LVTTL applications.

Voltage levels and margins, Rpol = 560 ohm 1/4 W, R = 180 ohm 1/8W.

Isolated Output Logic Level	Isolated Output State	Isolated Output Voltage Level	TTL Input Voltage Level	Voltage Margin	TTL Input Logic Level
High	Close	2.7 V max (2)	2.0 V min	0.7 V	High
Low	Open	0.36 V max (1)	0.8 V max	0.44 V	Low

Refer to "Isolated Output" on page 26 for voltage levels of isolated outputs.

Note 1 0.36V is obtained considering a worst-case external (pull-up) load of 2 mA (180 ohm x 2 mA = 0.36V), which means that the circuit can support the presence of an external pull-up resistor up to a (minimum) value of 1K5 ohm (in 3.3V) or 2K4 ohm (in 5V). If needed, an other R value can be chosen according to the actual pull-up load within the circuit.

Note 2 R_{POL} limits the Voh voltage to about 2.7V in order to match TTL and LVTTL levels. 2.7 V is obtained considering the R_{POL}-R 560 ohm-180 ohm divider and taking into account that the voltage drop across the opto-coupler pins ($V_{OUT}{}^{+}$ - $V_{OUT}t^{-}$) is about 0.9V.

Dynamic Limitations

The maximum pulse width of isolated outputs is about 5 µs and the maximum pulse rate is 100 KHz,

Isolated outputs add an extra delay of about 5 µs in the signal propagation.

The resistor value of R = 180 ohm has good dynamic results for a usual capacitive loads as 1 or 2 meters of cable. As example, a 2m cable will add 100 pF of load (50pF/m) which give a rise time of about 18 µs at 180 ohm (R x C = 180 ohm x 100 pF = 18 µs) . If needed, the R value can be adapted to match special requirements in terms of rise time and/or capacitive load.

If maximizing the opto-coupler switching time is a concern, it is not recommended to not increase too much the value of the resistor. The opto-coupler circuit behaves better (switching times) with a load of about 10 mA or higher. R = 180 ohm loads the opto-coupler at 13 mA (3.3V) and 23 mA (5V).

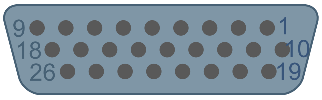
1.4. Coaxlink I/O Connectors

External I/O Connector

Applies to: Mono Duo Quad QuadG3 QuadCXP3 Quad3DLLE

Connector description

Property	Value
Name	External I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN12+	High-speed differential input #12 – Positive pole
3	IIN11+	Isolated input #11 – Positive pole
4	IIN13-	Isolated input #13 – Negative pole
5	IIN14-	Isolated input #14 – Negative pole
6	IOUT12-	Isolated contact output #12 – Negative pole
7	GND	Ground
8		Not connected
9	GND	Ground
10	GND	Ground
11	DIN12-	High-speed differential input #12 – Negative pole
12	IIN11-	Isolated input #11 – Negative pole
13	IIN12+	Isolated input #12 – Positive pole
14	IIN13+	Isolated input #13 – Positive pole
15	IIN14+	Isolated input #14 – Positive pole

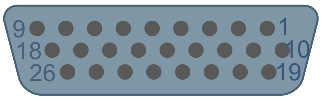
Pin	Signal	Usage
16	IOUT12+	Isolated contact output #12 – Positive pole
17	TTLIO12	TTL input/output #12
18	GND	Ground
19	DIN11-	High-speed differential input #11 – Negative pole
20	DIN11+	High-speed differential input #11 – Positive pole
21	IIN12-	Isolated input #12 – Negative pole
22	IOUT11-	Isolated contact output #11 – Negative pole
23	IOUT11+	Isolated contact output #11 – Positive pole
24	GND	Ground
25	TTLIO11	TTL input/output #11
26	+12V	+12 V Power output

I/O Connector

Applies to: Duo104EMB

Connector description

Property	Value
Name	I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Remote I/O module
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN12+	High-speed differential input #12 – Positive pole
3	IIN11+	Isolated input #11 – Positive pole
4	IIN13-	Isolated input #13 – Negative pole
5	IIN14-	Isolated input #14 – Negative pole
6	IOUT12-	Isolated contact output #12 – Negative pole
7	GND	Ground
8		Not connected
9	GND	Ground
10	GND	Ground
11	DIN12-	High-speed differential input #12 – Negative pole
12	IIN11-	Isolated input #11 – Negative pole
13	IIN12+	Isolated input #12 – Positive pole
14	IIN13+	Isolated input #13 – Positive pole
15	IIN14+	Isolated input #14 – Positive pole

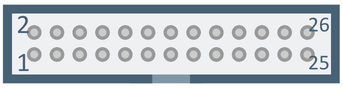
Pin	Signal	Usage
16	IOUT12+	Isolated contact output #12 – Positive pole
17	TTLIO12	TTL input/output #12
18	GND	Ground
19	DIN11-	High-speed differential input #11 – Negative pole
20	DIN11+	High-speed differential input #11 – Positive pole
21	IIN12-	Isolated input #12 – Negative pole
22	IOUT11-	Isolated contact output #11 – Negative pole
23	IOUT11+	Isolated contact output #11 – Positive pole
24	GND	Ground
25	TTLIO11	TTL input/output #11
26	+12V	+12 V Power output

Internal I/O 1 Connector

Applies to: Mono Duo Quad QuadG3 QuadG3DF QuadCXP3 Quad3DLLE Octo

Connector description

Property	Value
Name	Internal I/O 1
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN11+	High-speed differential input #11 – Positive pole
4	DIN11-	High-speed differential input #11 – Negative pole
5	DIN12+	High-speed differential input #12 – Positive pole
6	DIN12-	High-speed differential input #12 – Negative pole
7	IIN11+	Isolated input #11 – Positive pole
8	IIN11-	Isolated input #11 – Negative pole
9	IIN12+	Isolated input #12 – Positive pole
10	IIN12-	Isolated input #12 – Negative pole
11	IIN13+	Isolated input #13 – Positive pole
12	IIN13-	Isolated input #13 – Negative pole
13	IIN14+	Isolated input #14 – Positive pole
14	IIN14-	Isolated input #14 – Negative pole
15	IOUT11+	Isolated contact output #11 – Positive pole

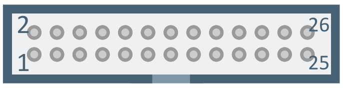
Pin	Signal	Usage
16	IOUT11-	Isolated contact output #11 – Negative pole
17	IOUT12+	Isolated contact output #12 – Positive pole
18	IOUT12-	Isolated contact output #12 – Negative pole
19	TTLIO11	TTL input/output #11
20	GND	Ground
21	TTLIO12	TTL input/output #12
22	GND	Ground
23		Not connected
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

Internal I/O 2 Connector

Applies to: Duo Quad QuadG3 QuadCXP3 Quad3DLLE

Connector description

Property	Value
Name	Internal I/O 2
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output



Pin assignments

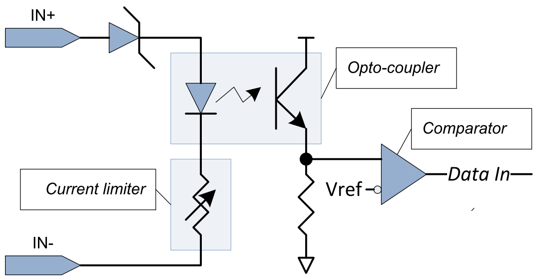
Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN21+	High-speed differential input #21 – Positive pole
4	DIN21-	High-speed differential input #21 – Negative pole
5	DIN22+	High-speed differential input #22 – Positive pole
6	DIN22-	High-speed differential input #22 – Negative pole
7	IIN21+	Isolated input #21 – Positive pole
8	IIN21-	Isolated input #21 – Negative pole
9	IIN22+	Isolated input #22 – Positive pole
10	IIN22-	Isolated input #22 – Negative pole
11	IIN23+	Isolated input #23 – Positive pole
12	IIN23-	Isolated input #23 – Negative pole
13	IIN24+	Isolated input #24 – Positive pole
14	IIN24-	Isolated input #24 – Negative pole
15	IOUT21+	Isolated contact output #21 – Positive pole

Pin	Signal	Usage
16	IOUT21-	Isolated contact output #21 – Negative pole
17	IOUT22+	Isolated contact output #22 – Positive pole
18	IOUT22-	Isolated contact output #22 – Negative pole
19	TTLIO21	TTL input/output #21
20	GND	Ground
21	TTLIO22	TTL input/output #22
22	GND	Ground
23		Not connected
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

1.5. Isolated I/O Specification

Isolated Input

Specification of the isolated GPIO input ports

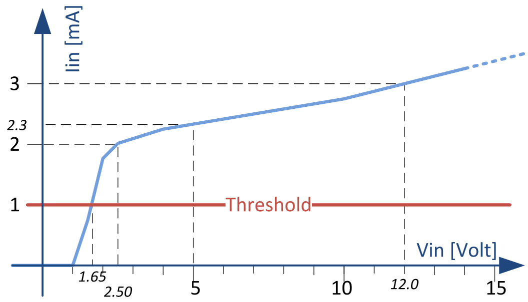


Isolated Input Simplified schematic

The input port implements an isolated current-sense input.

DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential voltage		-30		+30	V
Input current threshold			1		mA
Differential voltage	@1 mA	1.5	1.65	1.9	V
Input current	@(VIN+ - VIN-) = 1.65 V		1		mA
	@(VIN+ - VIN-) = 2.5 V		2		mA
	@(VIN+ - VIN-) = 5 V		2.3		mA
	@(VIN+ - VIN-) = 12 V		3		mA
	@(VIN+ - VIN-) = 30 V			5	mA
	@(VIN+ - VIN-) < 1 V			10	µA
DC isolation voltage		250			V
AC isolation voltage		170			V_{RMS}



Input Current vs. Input Voltage Characteristics

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	10			µs
Pulse rate	0		50	kHz

Logical map

The state of the port is reported as follows:

Input current	Logical State
IIN > 1 mA	HIGH
IIN < 1 mA	LOW
Unconnected input port	LOW

Compatible drivers and receivers

The following drivers are compatible with the isolated current-sense inputs:

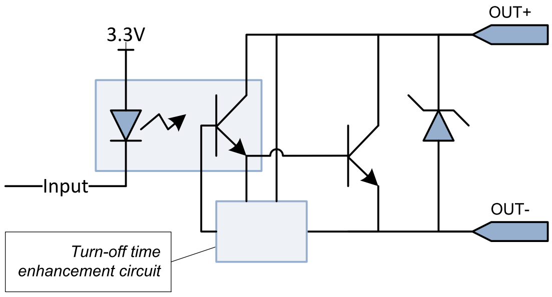
- Totem-pole LVTTL, TTL, 5 V CMOS drivers
- RS-422 Differential line drivers
- Potential free contact, solid-state relay, or opto-isolators
- 12 V and 24 V signaling voltages are also accepted

  Note: *The +12 V power supply on the I/O connector(s) can be used for powering drivers requiring a power supply.*

  Note: *No external resistors are required. However, to obtain the best noise immunity with 12 V and 24 V signaling, it is recommended to insert a series resistor in the circuit. The recommended resistor values are: 4.7k Ohms for 12 V signaling and 10k Ohms for 24 V signaling.*

Isolated Output

Specification of the isolated GPIO output ports



Isolated Output Simplified schematic

The output port implements an isolated contact output.

DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Current				100	mA
Differential voltage	Open state	-30		30	V
	Closed state @ 1 mA			0.4	V
	Closed state @ 100 mA			1.0	V
DC isolation voltage		250			V
AC isolation voltage		170			V_{RMS}

Note: *The output port in the closed state has no current limiter, the user circuit must be designed to avoid excessive currents that could destroy the output port.*

Note: *The output port remains in the OFF-state until it is under control of the application.*

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse rate	0		100	kHz
Turn-on time			5	µs
Turn-off time			5	µs

Typical switching performance @ 25°C

Current [mA]	Turn ON time [µs]	Turn OFF time [µs]
0.5	2.0	4.8
1.0	2.0	3.9
4.0	2.2	3.3
10	2.3	2.7
40	2.3	2.7
100	2.3	2.7

Logical map

The state of the output port is determined as follows:

Logical State	Output port state
HIGH	The contact switch is closed (ON)
LOW	The contact switch is open (OFF)

Compatible loads

The following loads are compatible with the isolated contact output ports:

- Any load within the 30V / 100 mA envelope is accepted. The power originates from an external power source or alternatively from the power delivered through the 12V and GND pins of the I/O connectors.