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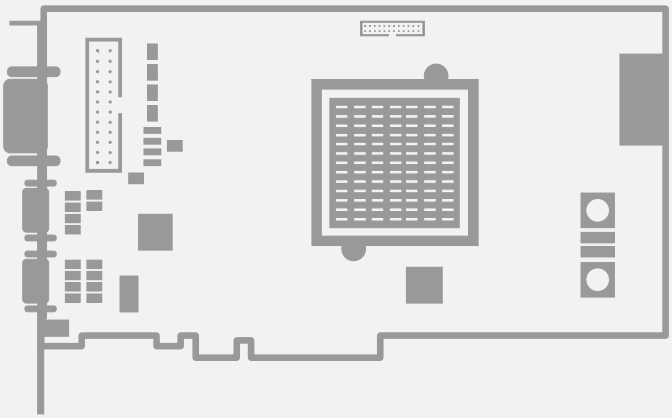
Empowering Computer Vision

HARDWARE MANUAL

Grablink

Grablink Hardware Manual

1622 Grablink Full
1623 Grablink DualBase
1624 Grablink Base
1626 Grablink Full XR



This documentation is provided with **Grablink 6.19.0** (doc build **4054**).
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1. About This Document

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1.1. Document Scope

This document describes the **hardware specifications** of all the products of the Grablink series together with their related products.

Grablink main products

Product	S/N Prefix	Icon
1622 Grablink Full	FM1	Full
1623 Grablink DualBase	GDB	DualBase
1624 Grablink Base	GBA	Base
1626 Grablink Full XR	FXR	FullXR

Grablink accessories

Product	S/N Prefix	Icon
1625 DB25F I/O Adapter Cable	DBC	1625
3304 HD26F I/O Adapter Cable		3304
3305 C2C SyncBus Cable		3305
3306 C2C Quad SyncBus Cable		3306

NOTE
The S/N prefix is a 3-letter string at the beginning of the card serial number.

NOTE
Icons are used in this document for tagging titles of card-specific content.

1.2. Document Structure

This document is composed of 4 main sections:

- "Mechanical Specification" on page 6 provides the product pictures, the physical dimensions, the connectors description and the pin assignments, the lamps description, etc.
- "Electrical Specification" on page 47 provides the electrical characteristics of all input/output ports, a description of the power distribution, power requirements, etc.
- "Environmental Specification" on page 77 provides the climatic requirements and CE/FCC/RoHS/WEEE compliance statements.
- "Related Products & Accessories" on page 81 provides a description of related products and accessories such as adapters, cables...

1.3. Document Changes

MultiCam 6.18

The following topic was revised:

- "IIN* Isolated Current-Sense Input Ports" on page 65

2. Mechanical Specification

Mechanical specifications of the product(s) including: product pictures, physical dimensions, connectors description and pin assignments, LEDs description, switches description, etc.

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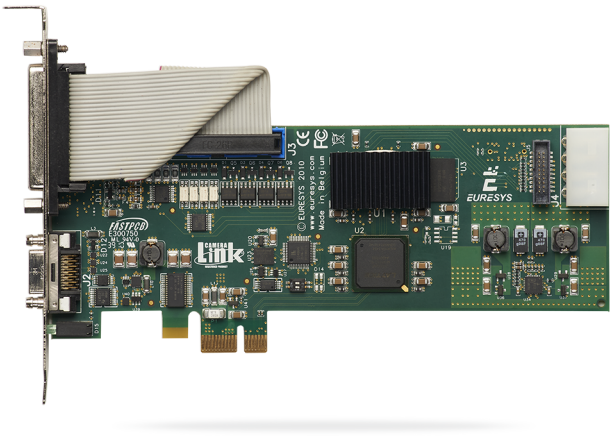
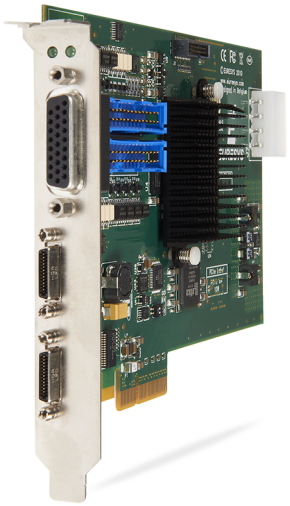
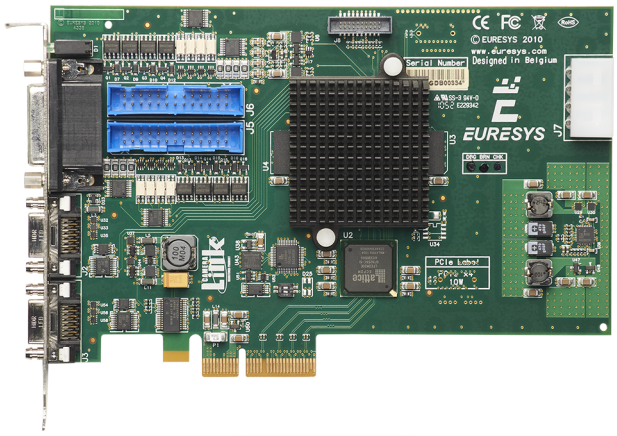
2.1. Product Pictures

1624 Grablink Base

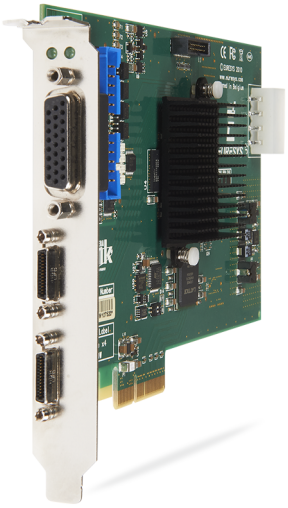


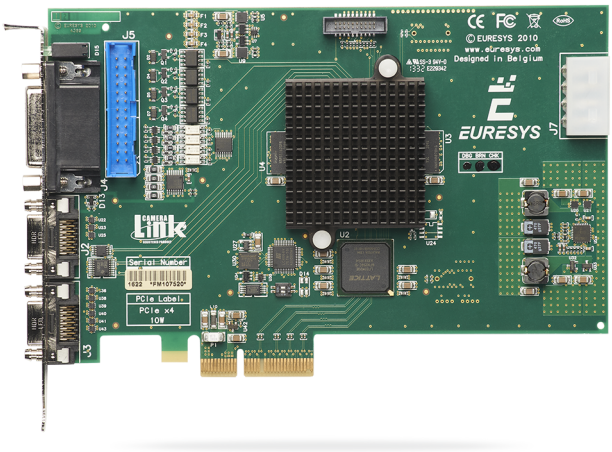
1623 Grablink DualBase



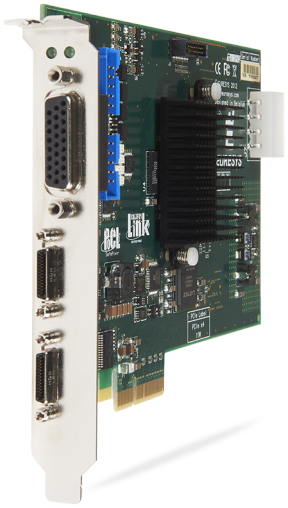


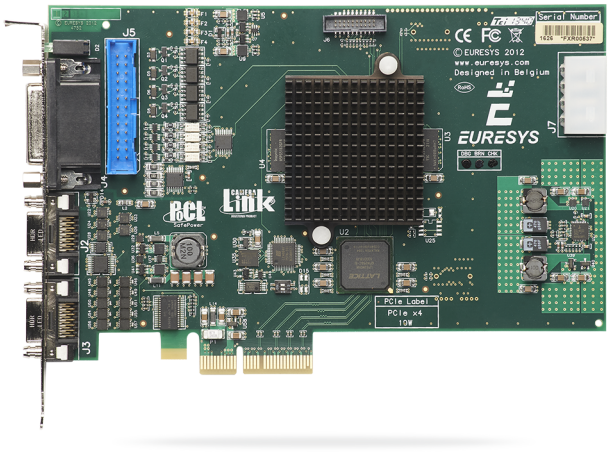
1622 Grablink Full





1626 Grablink Full XR





2.2. Physical Characteristics

Dimensions and Weight

Grablink Products

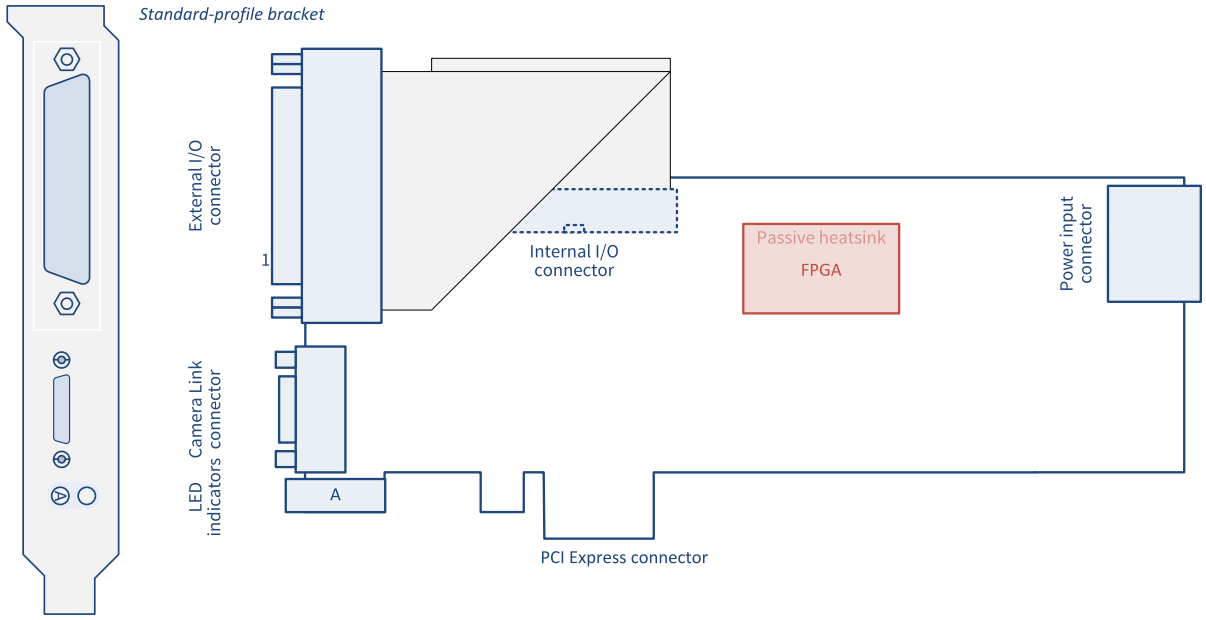
Product	Length	Height	Weight
1622 Grablink Full	167.5 mm, 6.6 in	111.15 mm, 4.38 in	133 g, 4.69 oz
1623 Grablink DualBase	167.5 mm, 6.6 in	111.15 mm, 4.38 in	137 g, 4.83 oz
1624 Grablink Base	167.5 mm, 6.6 in	68.9 mm, 2.71 in	98 g, 3.46 oz
1626 Grablink Full XR	167.5 mm, 6.6 in	111.15 mm, 4.38 in	136 g, 4.80 oz

2.3. Board and Bracket Layouts

1624 Grablink Base 11
1623 Grablink DualBase 13
1622 Grablink Full 14
1626 Grablink Full XR 15

1624 Grablink Base

Factory default assembly for standard-profile chassis



The **1624 Grablink Base** board is fitted at factory with a standard profile bracket having 2 connectors and 2 LED indicators:

- The upper connector, called "External I/O Connector" on page 31, is for system connection, such as external trigger, illumination control or motion encoder.
- The lower connector, called "Camera Link Connector" on page 17, is for the connection of a Camera Link Base camera. It complies with the Camera Link standard Shrunk Delta Ribbon - SDR - connector and supports PoCL.
- At the lowest end, the "LED Indicators" on page 46 report board and acquisition status.

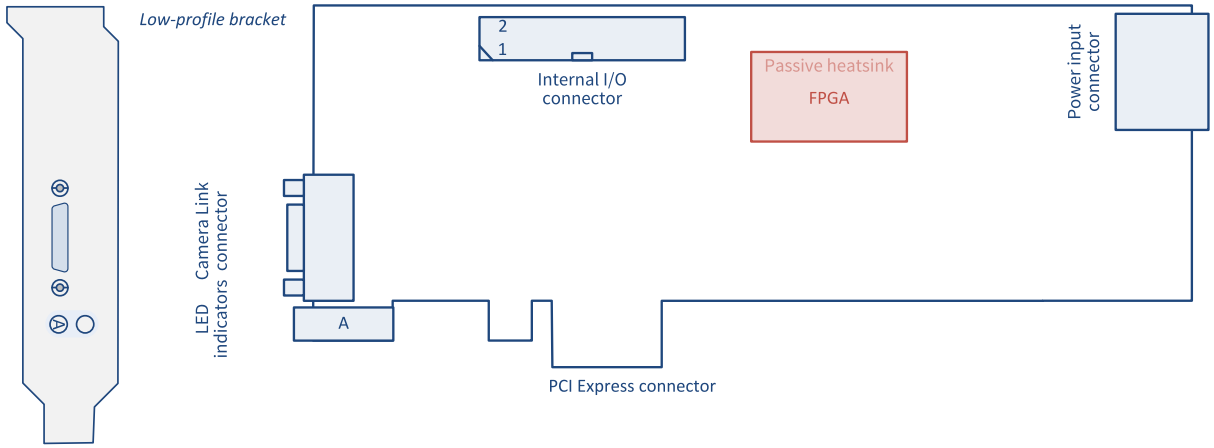
The **1624 Grablink Base** board is fitted, at factory exit, with 2 internal connectors:

- The "Internal I/O Connector" on page 37 is for system connection, such as external trigger, illumination control or motion encoder. It is connected to the "External I/O Connector" on page 31 with a flat cable.
- The "Power Input Connector" on page 43 is for powering the camera through PoCL and powering system devices through the I/O connectors.

Alternate assembly for low-profile chassis

1624 Grablink Base comes with two parts: a standard-profile board assembly (board + standard-profile bracket) and an extra low-profile bracket.

The standard-profile board assembly can be converted into a low-profile board assembly by exchanging the original bracket with the low-profile bracket.Therefore , remove the original standard-profile bracket by using a flat screwdriver, and re-install the screw locks of the Camera Link connector.



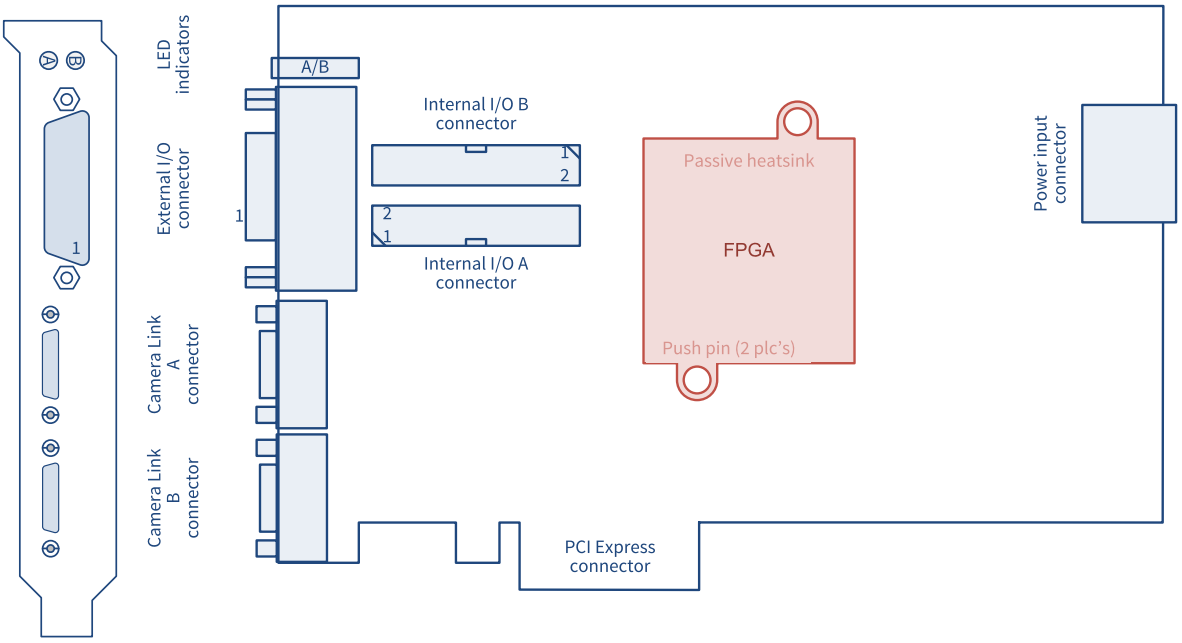
The low-profile bracket has 1 connector and 2 LED indicators:

- The connector, called "Camera Link Connector" on page 17 , is for the connection of a Camera Link Base camera. It complies with the Camera Link standard Shrunk Delta Ribbon - SDR - connector and supports PoCL.
- At the lowest end, the "LED Indicators" on page 46 report board and acquisition status.

The **1624 Grablink Base** board is fitted, with 2 internal connectors:

- The "Internal I/O Connector" on page 37 is for system connection, such as external trigger, illumination control or motion encoder.
- The "Power Input Connector" on page 43 is for powering the camera through PoCL and powering system devices through the I/O connectors.

1623 Grablink DualBase



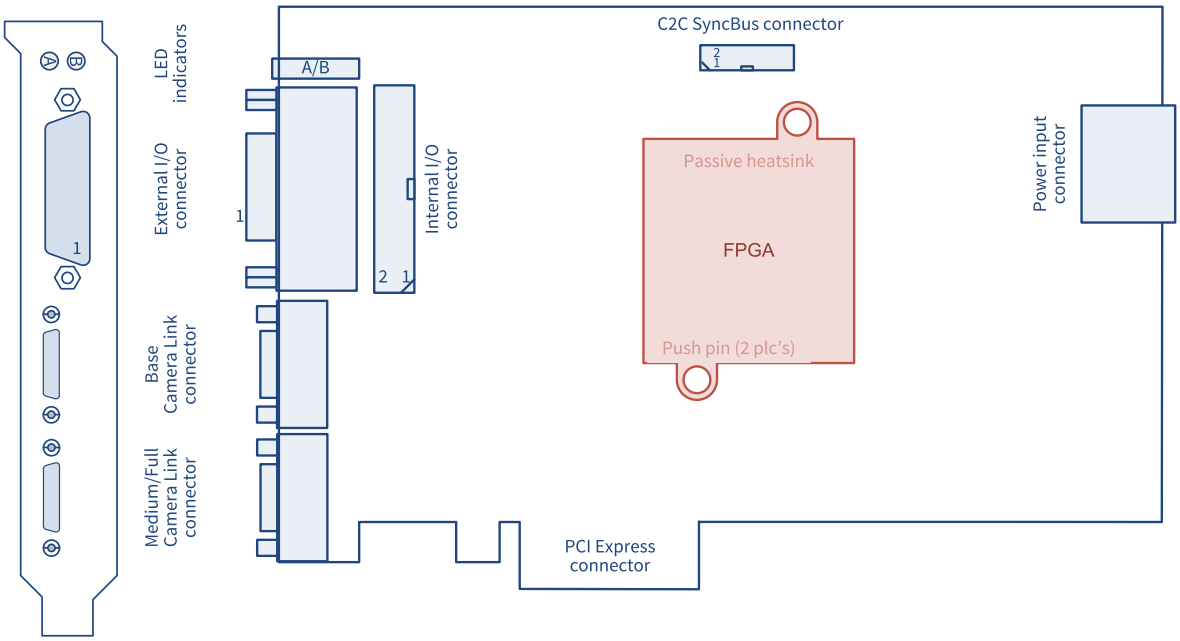
The **1623 Grablink DualBase** board is fitted with a standard profile bracket having 2 LED indicators and 3 connectors

- At the upper end, the "LED Indicators" on page 46 report board and acquisition status for Channel A and Channel B respectively.
- The upper connector, called "External I/O Connector" on page 33, is for system connection, such as external trigger, illumination control or motion encoder.
- The center connector, called "Camera Link A Connector" on page 19, is for the connection of a single-cable Base camera feeding the Channel A. It complies with the Camera Link standard Shrunk Delta Ribbon - SDR - connector and supports PoCL.
- The lower connector, called "Camera Link B Connector" on page 21, is for the connection of another single-cable Base camera feeding the Channel B. It complies with the Camera Link standard Shrunk Delta Ribbon - SDR - connector and supports PoCL.

The **1623 Grablink DualBase** board is fitted, at factory exit, with 3 internal connectors:

- The "Channel A Internal I/O Connector" on page 39 is for system connection, such as external trigger, illumination control or motion encoder related to Channel A.
- The "Channel B Internal I/O Connector" on page 41 is for system connection, such as external trigger, illumination control or motion encoder related to Channel B.
- The "Power Input Connector" on page 43 is for powering the cameras through PoCL and powering system devices through the I/O connectors.

1622 Grablink Full



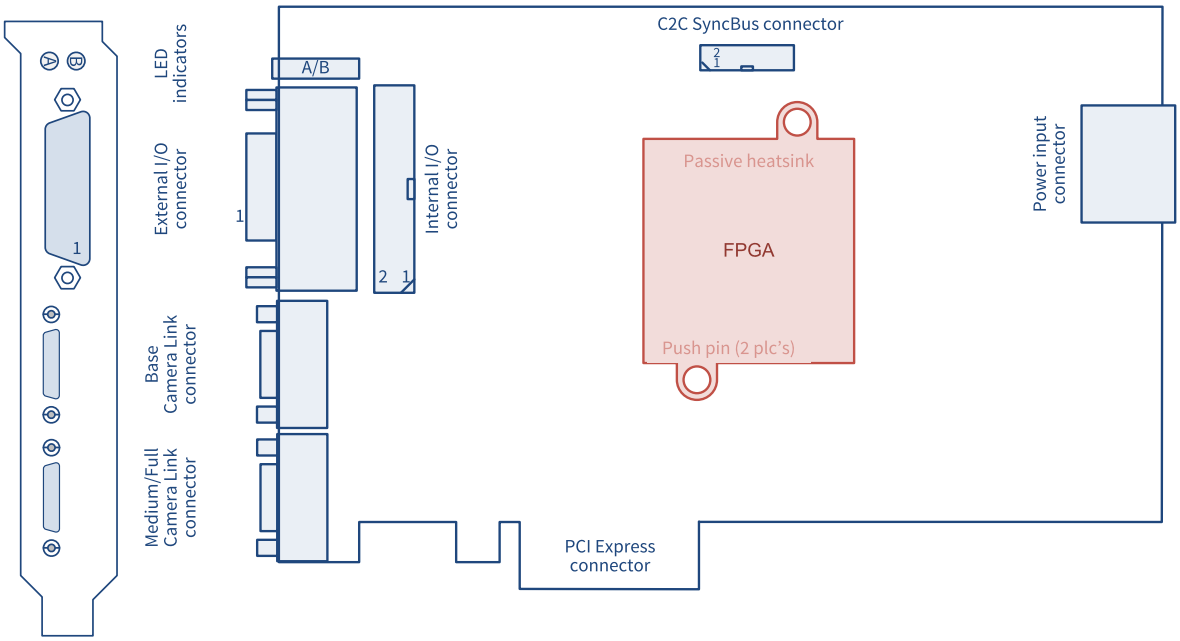
The **1622 Grablink Full** board is fitted with a standard profile bracket having 2 LED indicators and 3 connectors

- The upper connector, called "External I/O Connector" on page 35, is for system connection, such as external trigger, illumination control or motion encoder.
- The center connector, called "Base Camera Link Connector" on page 23 connector, is for the connection of a single-cable Base camera and the first cable of a Medium-, Full- or 80-bit camera. It complies with the Camera Link standard Shrunk Delta Ribbon - SDR - connector.
- The lower connector, called "Medium/Full Camera Link Connector" on page 25 connector, is for the connection of the second cable of a Medium-, Full- or 80-bit camera. It complies with the Camera Link standard Shrunk Delta Ribbon - SDR - connector.

The **1622 Grablink Full** board is fitted with 3 internal connectors:

- The "Internal I/O Connector" on page 37 is for system connection, such as external trigger, illumination control or motion encoder.
- The "Power Input Connector" on page 43 is for powering system devices through the I/O connectors.
- The "C2C SyncBus Connector" on page 45 is for the synchronization of two **1622 Grablink Full** or **1626 Grablink Full XR** cards.

1626 Grablink Full XR



The **1626 Grablink Full XR** board is fitted with a standard profile bracket having 2 LED indicators and 3 connectors

- The upper connector, called "External I/O Connector" on page 35, is for system connection, such as external trigger, illumination control or motion encoder.
- The center connector, called "Base Camera Link Connector" on page 27 connector, is for the connection of a single-cable Base camera and the first cable of a Medium-, Full- or 80-bit camera. It complies with the Camera Link standard Shrunk Delta Ribbon - SDR - connector and supports PoCL.
- The lower connector, called "Medium/Full Camera Link Connector" on page 29 connector, is for the connection of the second cable of a Medium-, Full- or 80-bit camera. It complies with the Camera Link standard Shrunk Delta Ribbon - SDR - connector and supports PoCL.

The **1626 Grablink Full XR** board is fitted with 3 internal connectors:

- The "Internal I/O Connector" on page 37 is for system connection, such as external trigger, illumination control or motion encoder.
- The "Power Input Connector" on page 43 is for powering the cameras through PoCL and powering system devices through the I/O connectors.
- The "C2C SyncBus Connector" on page 45 is for the synchronization of two **1622 Grablink Full** or **1626 Grablink Full XR** cards.

2.4. Connectors

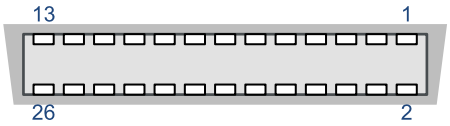
Camera Link Connector 17
Camera Link A Connector 19
Camera Link B Connector 21
Base Camera Link Connector 23
Medium/Full Camera Link Connector 25
Base Camera Link Connector 27
Medium/Full Camera Link Connector 29
External I/O Connector 31
External I/O Connector 33
External I/O Connector 35
Internal I/O Connector 37
Channel A Internal I/O Connector 39
Channel B Internal I/O Connector 41
Power Input Connector 43
Power Input Connector 44
C2C SyncBus Connector 45

Camera Link Connector

Applies to: Base

Connector description

Property	Value
Name	Camera Link
Type	26-position Shrunk Delta Ribbon socket
Location	Card bracket
Usage	PoCL Camera Link camera input



Pin assignments

Pin	Signal	Usage
1	PoCL	PoCL #1 +12V Power output
2	CC4-	Camera Control 4 – Negative pole
3	CC3+	Camera Control 3 – Positive pole
4	CC2-	Camera Control 2 – Negative pole
5	CC1+	Camera Control 1 – Positive pole
6	SERTFG+	Serial COM to Frame Grabber – Positive pole
7	SERTC-	Serial COM to Camera – Negative pole
8	X3+	Channel Link X – Pair 3 – Positive pole
9	XCLK+	Channel Link X – Clock – Positive pole
10	X2+	Channel Link X – Pair 2 – Positive pole
11	X1+	Channel Link X – Pair 1 – Positive pole
12	X0+	Channel Link X – Pair 0 – Positive pole
13	GND	Ground
14	GND	Ground
15	CC4+	Camera Control 4 – Positive pole
16	CC3-	Camera Control 3 – Negative pole
17	CC2+	Camera Control 2 – Positive pole

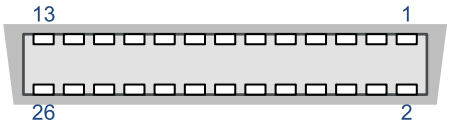
Pin	Signal	Usage
18	CC1-	Camera Control 1 – Negative pole
19	SERTFG-	Serial COM to Frame Grabber – Negative pole
20	SERTC+	Serial COM to Camera – Positive pole
21	X3-	Channel Link X – Pair 3 – Negative pole
22	XCLK-	Channel Link X – Clock – Negative pole
23	X2-	Channel Link X – Pair 2 – Negative pole
24	X1-	Channel Link X – Pair 1 – Negative pole
25	X0-	Channel Link X – Pair 0 – Negative pole
262	PoCL	PoCL #1 +12V Power output

Camera Link A Connector

Applies to: DualBase

Connector description

Property	Value
Name	Camera Link A
Type	26-position Shrunk Delta Ribbon socket
Location	Card bracket
Usage	Channel A PoCL Camera Link camera input



Pin assignments

Pin	Signal	Usage
1	PoCL	PoCL #1 +12V Power output
2	CC4-	Camera Control 4 – Negative pole
3	CC3+	Camera Control 3 – Positive pole
4	CC2-	Camera Control 2 – Negative pole
5	CC1+	Camera Control 1 – Positive pole
6	SERTFG+	Serial COM to Frame Grabber – Positive pole
7	SERTC-	Serial COM to Camera – Negative pole
8	X3+	Channel Link X – Pair 3 – Positive pole
9	XCLK+	Channel Link X – Clock – Positive pole
10	X2+	Channel Link X – Pair 2 – Positive pole
11	X1+	Channel Link X – Pair 1 – Positive pole
12	X0+	Channel Link X – Pair 0 – Positive pole
13	GND	Ground
14	GND	Ground
15	CC4+	Camera Control 4 – Positive pole
16	CC3-	Camera Control 3 – Negative pole
17	CC2+	Camera Control 2 – Positive pole

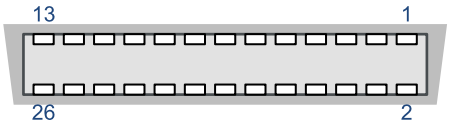
Pin	Signal	Usage
18	CC1-	Camera Control 1 – Negative pole
19	SERTFG-	Serial COM to Frame Grabber – Negative pole
20	SERTC+	Serial COM to Camera – Positive pole
21	X3-	Channel Link X – Pair 3 – Negative pole
22	XCLK-	Channel Link X – Clock – Negative pole
23	X2-	Channel Link X – Pair 2 – Negative pole
24	X1-	Channel Link X – Pair 1 – Negative pole
25	X0-	Channel Link X – Pair 0 – Negative pole
262	PoCL	PoCL #1 +12V Power output

Camera Link B Connector

Applies to: DualBase

Connector description

Property	Value
Name	Camera Link B
Type	26-position Shrunk Delta Ribbon socket
Location	Card bracket
Usage	Channel B PoCL Camera Link camera input



Pin assignments

Pin	Signal	Usage
1	PoCL	PoCL #1 +12V Power output
2	CC4-	Camera Control 4 – Negative pole
3	CC3+	Camera Control 3 – Positive pole
4	CC2-	Camera Control 2 – Negative pole
5	CC1+	Camera Control 1 – Positive pole
6	SERTFG+	Serial COM to Frame Grabber – Positive pole
7	SERTC-	Serial COM to Camera – Negative pole
8	X3+	Channel Link X – Pair 3 – Positive pole
9	XCLK+	Channel Link X – Clock – Positive pole
10	X2+	Channel Link X – Pair 2 – Positive pole
11	X1+	Channel Link X – Pair 1 – Positive pole
12	X0+	Channel Link X – Pair 0 – Positive pole
13	GND	Ground
14	GND	Ground
15	CC4+	Camera Control 4 – Positive pole
16	CC3-	Camera Control 3 – Negative pole
17	CC2+	Camera Control 2 – Positive pole

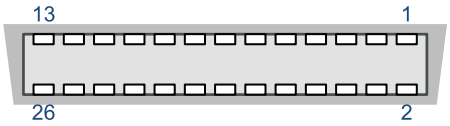
Pin	Signal	Usage
18	CC1-	Camera Control 1 – Negative pole
19	SERTFG-	Serial COM to Frame Grabber – Negative pole
20	SERTC+	Serial COM to Camera – Positive pole
21	X3-	Channel Link X – Pair 3 – Negative pole
22	XCLK-	Channel Link X – Clock – Negative pole
23	X2-	Channel Link X – Pair 2 – Negative pole
24	X1-	Channel Link X – Pair 1 – Negative pole
25	X0-	Channel Link X – Pair 0 – Negative pole
262	PoCL	PoCL #1 +12V Power output

Base Camera Link Connector

Applies to: Full

Connector description

Property	Value
Name	Base Camera Link
Type	26-position Shrunk Delta Ribbon socket
Location	Card bracket
Usage	Camera Link camera input (First cable)



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	CC4-	Camera Control 4 – Negative pole
3	CC3+	Camera Control 3 – Positive pole
4	CC2-	Camera Control 2 – Negative pole
5	CC1+	Camera Control 1 – Positive pole
6	SERTFG+	Serial COM to Frame Grabber – Positive pole
7	SERTC-	Serial COM to Camera – Negative pole
8	X3+	Channel Link X – Pair 3 – Positive pole
9	XCLK+	Channel Link X – Clock – Positive pole
10	X2+	Channel Link X – Pair 2 – Positive pole
11	X1+	Channel Link X – Pair 1 – Positive pole
12	X0+	Channel Link X – Pair 0 – Positive pole
13	GND	Ground
14	GND	Ground
15	CC4+	Camera Control 4 – Positive pole
16	CC3-	Camera Control 3 – Negative pole
17	CC2+	Camera Control 2 – Positive pole

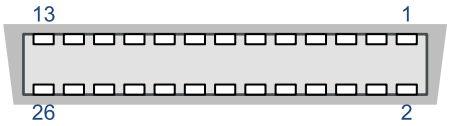
Pin	Signal	Usage
18	CC1-	Camera Control 1 – Negative pole
19	SERTFG-	Serial COM to Frame Grabber – Negative pole
20	SERTC+	Serial COM to Camera – Positive pole
21	X3-	Channel Link X – Pair 3 – Negative pole
22	XCLK-	Channel Link X – Clock – Negative pole
23	X2-	Channel Link X – Pair 2 – Negative pole
24	X1-	Channel Link X – Pair 1 – Negative pole
25	X0-	Channel Link X – Pair 0 – Negative pole
262	GND	Ground

Medium/Full Camera Link Connector

Applies to: Full

Connector description

Property	Value
Name	Medium/Full Camera Link
Type	26-position Shrunk Delta Ribbon socket
Location	Card bracket
Usage	Camera Link camera input (Second cable)



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	Z3+	Channel Link Z – Pair 3 – Positive pole
3	ZCLK+	Channel Link Z – Clock – Positive pole
4	Z2+	Channel Link Z – Pair 2 – Positive pole
5	Z1+	Channel Link Z – Pair 1 – Positive pole
6	Z0+	Channel Link Z – Pair 0 – Positive pole
7	TERM-	Unused but terminated pair
8	Y3+	Channel Link Y – Pair 3 – Positive pole
9	YCLK+	Channel Link Y – Clock – Positive pole
10	Y2+	Channel Link Y – Pair 2 – Positive pole
11	Y1+	Channel Link Y – Pair 1 – Positive pole
12	Y0+	Channel Link Y – Pair 0 – Positive pole
13	GND	Ground
14	GND	Ground
15	Z3-	Channel Link Z – Pair 3 – Negative pole
16	ZCLK-	Channel Link Z – Clock – Negative pole
17	Z2-	Channel Link Z – Pair 2 – Negative pole

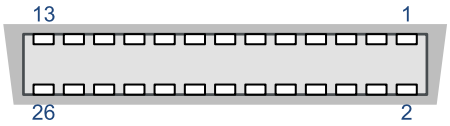
Pin	Signal	Usage
18	Z1-	Channel Link Z – Pair 1 – Negative pole
19	Z0-	Channel Link Z – Pair 0 – Negative pole
20	TERM+	Unused but terminated pair
21	Y3-	Channel Link Y – Pair 3 – Negative pole
22	YCLK-	Channel Link Y – Clock – Negative pole
23	Y2-	Channel Link Y – Pair 2 – Negative pole
24	Y1-	Channel Link Y – Pair 1 – Negative pole
25	Y0-	Channel Link Y – Pair 0 – Negative pole
262	GND	Ground

Base Camera Link Connector

Applies to: FullXR

Connector description

Property	Value
Name	Base Camera Link
Type	26-position Shrunk Delta Ribbon socket
Location	Card bracket
Usage	PoCL Camera Link camera input (First cable)



Pin assignments

Pin	Signal	Usage
1	PoCL	PoCL #1 +12V Power output
2	CC4-	Camera Control 4 – Negative pole
3	CC3+	Camera Control 3 – Positive pole
4	CC2-	Camera Control 2 – Negative pole
5	CC1+	Camera Control 1 – Positive pole
6	SERTFG+	Serial COM to Frame Grabber – Positive pole
7	SERTC-	Serial COM to Camera – Negative pole
8	X3+	Channel Link X – Pair 3 – Positive pole
9	XCLK+	Channel Link X – Clock – Positive pole
10	X2+	Channel Link X – Pair 2 – Positive pole
11	X1+	Channel Link X – Pair 1 – Positive pole
12	X0+	Channel Link X – Pair 0 – Positive pole
13	GND	Ground
14	GND	Ground
15	CC4+	Camera Control 4 – Positive pole
16	CC3-	Camera Control 3 – Negative pole
17	CC2+	Camera Control 2 – Positive pole

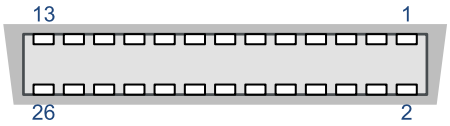
Pin	Signal	Usage
18	CC1-	Camera Control 1 – Negative pole
19	SERTFG-	Serial COM to Frame Grabber – Negative pole
20	SERTC+	Serial COM to Camera – Positive pole
21	X3-	Channel Link X – Pair 3 – Negative pole
22	XCLK-	Channel Link X – Clock – Negative pole
23	X2-	Channel Link X – Pair 2 – Negative pole
24	X1-	Channel Link X – Pair 1 – Negative pole
25	X0-	Channel Link X – Pair 0 – Negative pole
262	PoCL	PoCL #1 +12V Power output

Medium/Full Camera Link Connector

Applies to: FullXR

Connector description

Property	Value
Name	Medium/Full Camera Link
Type	26-position Shrunk Delta Ribbon socket
Location	Card bracket
Usage	PoCL Camera Link camera input (Second cable)



Pin assignments

Pin	Signal	Usage
1	PoCL	PoCL #2 +12V Power output
2	Z3+	Channel Link Z – Pair 3 – Positive pole
3	ZCLK+	Channel Link Z – Clock – Positive pole
4	Z2+	Channel Link Z – Pair 2 – Positive pole
5	Z1+	Channel Link Z – Pair 1 – Positive pole
6	Z0+	Channel Link Z – Pair 0 – Positive pole
7	TERM-	Unused but terminated pair
8	Y3+	Channel Link Y – Pair 3 – Positive pole
9	YCLK+	Channel Link Y – Clock – Positive pole
10	Y2+	Channel Link Y – Pair 2 – Positive pole
11	Y1+	Channel Link Y – Pair 1 – Positive pole
12	Y0+	Channel Link Y – Pair 0 – Positive pole
13	GND	Ground
14	GND	Ground
15	Z3-	Channel Link Z – Pair 3 – Negative pole
16	ZCLK-	Channel Link Z – Clock – Negative pole
17	Z2-	Channel Link Z – Pair 2 – Negative pole

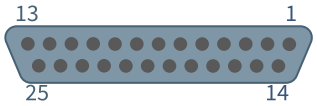
Pin	Signal	Usage
18	Z1-	Channel Link Z – Pair 1 – Negative pole
19	Z0-	Channel Link Z – Pair 0 – Negative pole
20	TERM+	Unused but terminated pair
21	Y3-	Channel Link Y – Pair 3 – Negative pole
22	YCLK-	Channel Link Y – Clock – Negative pole
23	Y2-	Channel Link Y – Pair 2 – Negative pole
24	Y1-	Channel Link Y – Pair 1 – Negative pole
25	Y0-	Channel Link Y – Pair 0 – Negative pole
262	PoCL	PoCL #1 +12V Power output

External I/O Connector

Applies to: Base

Connector description

Property	Value
Name	External I/O
Type	25-pin female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN1-	High-speed differential input #1 – Negative pole
3	DIN2-	High-speed differential input #2 – Negative pole
4	IIN1-	Isolated input #1 – Negative pole
5	IIN2-	Isolated input #2 – Negative pole
6	IIN3-	Isolated input #3 – Negative pole
7	IIN4-	Isolated input #4 – Negative pole
8	IOUT1-	Isolated contact output #1 – Negative pole
9	IOUT2-	Isolated contact output #2 – Negative pole
10	IOUT3-	Isolated contact output #3 – Negative pole
11	IOUT4-	Isolated contact output #4 – Negative pole
12	GND	Ground
13	GND	Ground
14	DIN1+	High-speed differential input #1 – Positive pole
15	DIN2+	High-speed differential input #2 – Positive pole
16	IIN1+	Isolated input #1 – Positive pole
17	IIN2+	Isolated input #2 – Positive pole

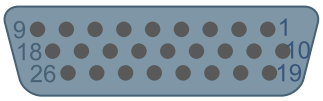
Pin	Signal	Usage
18	IIN3+	Isolated input #3 – Positive pole
19	IIN4+	Isolated input #4 – Positive pole
20	IOUT1+	Isolated contact output #1 – Positive pole
21	IOUT2+	Isolated contact output #2 – Positive pole
22	IOUT3+	Isolated contact output #3 – Positive pole
23	IOUT4+	Isolated contact output #4 – Positive pole
24	+5V	+5 V Power output
25	+12V	+12 V Power output
	+12V_RTN	Ground

External I/O Connector

Applies to: DualBase

Connector description

Property	Value
Name	External I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN2A+	Channel A - High-speed differential input #2 – Positive pole
3	IIN1A+	Channel A - Isolated input #1 – Positive pole
4	DIN1B-	Channel B - High-speed differential input #1 – Negative pole
5	DIN2B-	Channel B - High-speed differential input #2 – Negative pole
6	IIN1B-	Channel B - Isolated input #1 – Negative pole
7	IOUT1B-	Channel B -Isolated contact output #1 – Negative pole
8	+5V	+5V Power output
9	GND	Ground
10	GND	Ground
11	DIN2A-	Channel A - High-speed differential input #2 – Negative pole
12	IIN1A-	Channel A - Isolated input #1 – Negative pole
13	IIN2A+	Channel A - Isolated input #2 – Positive pole
14	DIN1B+	Channel B - High-speed differential input #1 – Positive pole
15	DIN2B+	Channel B - High-speed differential input #2 – Positive pole
16	IIN1B+	Channel B - Isolated input #1 – Positive pole
17	IOUT1B+	Channel B - Isolated contact output #1 – Positive pole

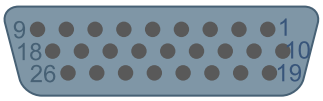
Pin	Signal	Usage
18	GND	Ground
19	DIN1A-	Channel A - High-speed differential input #1 – Negative pole
20	DIN1A+	Channel A - High-speed differential input #1 – Positive pole
21	IIN2A-	Channel A - Isolated input #2 – Negative pole
22	IOUT1A-	Channel A - Isolated contact output #1 – Negative pole
23	IOUT1A+	Channel A - Isolated contact output #1 – Positive pole
24	IIN2B-	Channel B - Isolated input #2 – Negative pole
25	IIN2B+	Channel B - Isolated input #2 – Positive pole
26	+12V	+12 V Power output

External I/O Connector

Applies to: Full FullXR

Connector description

Property	Value
Name	External I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN2+	High-speed differential input #2 – Positive pole
3	IIN1+	Isolated input #1 – Positive pole
4	IIN3-	Isolated input #3 – Negative pole
5	IIN4-	Isolated input #4 – Negative pole
6	IOUT2-	Isolated contact output #2 – Negative pole
7	IOUT4-	Isolated contact output #4 – Negative pole
8	+5V	+5V Power output
9	GND	Ground
10	GND	Ground
11	DIN2-	High-speed differential input #2 – Negative pole
12	IIN1-	Isolated input #1 – Negative pole
13	IIN2+	Isolated input #2 – Positive pole
14	IIN3+	Isolated input #3 – Positive pole
15	IIN4+	Isolated input #4 – Positive pole
16	IOUT2+	Isolated contact output #2 – Positive pole
17	IOUT4+	Isolated contact output #4 – Positive pole

Pin	Signal	Usage
18	GND	Ground
19	DIN1-	High-speed differential input #1 – Negative pole
20	DIN1+	High-speed differential input #1 – Positive pole
21	IIN2-	Isolated input #2 – Negative pole
22	IOUT1-	Isolated contact output #1 – Negative pole
23	IOUT1+	Isolated contact output #1 – Positive pole
24	IOUT3-	Isolated contact output #3 – Negative pole
25	IOUT3+	Isolated contact output #3 – Positive pole
26	+12V	+12 V Power output

Internal I/O Connector

Applies to: Base Full FullXR

Connector description

Property	Value
Name	Internal I/O
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output

Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN1+	High-speed differential input #1 – Positive pole
4	DIN1-	High-speed differential input #1 – Negative pole
5	DIN2+	High-speed differential input #2 – Positive pole
6	DIN2-	High-speed differential input #2 – Negative pole
7	IIN1+	Isolated input #1 – Positive pole
8	IIN1-	Isolated input #1 – Negative pole
9	IIN2+	Isolated input #2 – Positive pole
10	IIN2-	Isolated input #2 – Negative pole
11	IIN3+	Isolated input #3 – Positive pole
12	IIN3-	Isolated input #3 – Negative pole
13	IIN4+	Isolated input #4 – Positive pole
14	IIN4-	Isolated input #4 – Negative pole
15	IOUT1+	Isolated contact output #1 – Positive pole
16	IOUT1-	Isolated contact output #1 – Negative pole
17	IOUT2+	Isolated contact output #2 – Positive pole

Pin	Signal	Usage
18	IOUT2-	Isolated contact output #2 – Negative pole
19	IOUT3+	Isolated contact output #3 – Positive pole
20	IOUT3-	Isolated contact output #3 – Negative pole
21	IOUT4+	Isolated contact output #4 – Positive pole
22	IOUT4-	Isolated contact output #4 – Negative pole
23	+5V	+5 V Power output
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

Channel A Internal I/O Connector

Applies to: DualBase

Connector description

Property	Value
Name	Channel A Internal I/O
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output

Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN1A+	Channel A - High-speed differential input #1 – Positive pole
4	DIN1A-	Channel A - High-speed differential input #1 – Negative pole
5	DIN2A+	Channel A - High-speed differential input #2 – Positive pole
6	DIN2A-	Channel A - High-speed differential input #2 – Negative pole
7	IIN1A+	Channel A - Isolated input #1 – Positive pole
8	IIN1A-	Channel A - Isolated input #1 – Negative pole
9	IIN2A+	Channel A - Isolated input #2 – Positive pole
10	IIN2A-	Channel A - Isolated input #2 – Negative pole
11	IIN3A+	Channel A - Isolated input #3 – Positive pole
12	IIN3A-	Channel A - Isolated input #3 – Negative pole
13	IIN4A+	Channel A - Isolated input #4 – Positive pole
14	IIN4A-	Channel A - Isolated input #4 – Negative pole
15	IOUT1A+	Channel A - Isolated contact output #1 – Positive pole
16	IOUT1A-	Channel A - Isolated contact output #1 – Negative pole
17	IOUT2A+	Channel A - Isolated contact output #2 – Positive pole

Pin	Signal	Usage
18	IOUT2A-	Channel A - Isolated contact output #2 – Negative pole
19	IOUT3A+	Channel A - Isolated contact output #3 – Positive pole
20	IOUT3A-	Channel A - Isolated contact output #3 – Negative pole
21	IOUT4A+	Channel A - Isolated contact output #4 – Positive pole
22	IOUT4A-	Channel A - Isolated contact output #4 – Negative pole
23	+5V	+5 V Power output
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

Channel B Internal I/O Connector

Applies to: DualBase

Connector description

Property	Value
Name	Channel B Internal I/O
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output

Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN1B+	Channel B - High-speed differential input #1 – Positive pole
4	DIN1B-	Channel B - High-speed differential input #1 – Negative pole
5	DIN2B+	Channel B - High-speed differential input #2 – Positive pole
6	DIN2B-	Channel B - High-speed differential input #2 – Negative pole
7	IIN1B+	Channel B - Isolated input #1 – Positive pole
8	IIN1B-	Channel B - Isolated input #1 – Negative pole
9	IIN2B+	Channel B - Isolated input #2 – Positive pole
10	IIN2B-	Channel B - Isolated input #2 – Negative pole
11	IIN3B+	Channel B - Isolated input #3 – Positive pole
12	IIN3B-	Channel B - Isolated input #3 – Negative pole
13	IIN4B+	Channel B - Isolated input #4 – Positive pole
14	IIN4B-	Channel B - Isolated input #4 – Negative pole
15	IOUT1B+	Channel B - Isolated contact output #1 – Positive pole
16	IOUT1B-	Channel B - Isolated contact output #1 – Negative pole
17	IOUT2B+	Channel B - Isolated contact output #2 – Positive pole

Pin	Signal	Usage
18	IOUT2B-	Channel B - Isolated contact output #2 – Negative pole
19	IOUT3B+	Channel B - Isolated contact output #3 – Positive pole
20	IOUT3B-	Channel B - Isolated contact output #3 – Negative pole
21	IOUT4B+	Channel B - Isolated contact output #4 – Positive pole
22	IOUT4B-	Channel B - Isolated contact output #4 – Negative pole
23	+5V	+5 V Power output
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

Power Input Connector

Applies to: Base DualBase FullXR

Connector description

Property	Value
Name	Power Input
Type	4-pin Molex disk drive power male connector socket
Location	Printed circuit board
Usage	DC power input for PoCL and GPIO power output

Pin assignments

Pin	Signal	Usage
1	+12VIN	+12 V power input
2	GND	Ground
3	GND	Ground
4	+5VIN	+5 V power input

Power Input Connector

Applies to: Full

Connector description

Property	Value
Name	Power Input
Type	4-pin Molex disk drive power male connector socket
Location	Printed circuit board
Usage	DC power input for GPIO power output

Pin assignments

Pin	Signal	Usage
1	+12VIN	+12 V power input
2	GND	Ground
3	GND	Ground
4	+5VIN	+5 V power input

C2C SyncBus Connector

Applies to: Full FullXR

Connector description

Property	Value
Name	C2C SyncBus
Type	20-pin dual-row 0.050" pitch pin header with shrouding
Location	Printed circuit board
Usage	Card-to-card SyncBus

Pin assignments

Pin	Signal	Usage
3	GND	Ground
6	GND	Ground
7	GND	Ground
10	GND	Ground
17	C2C_1	Frame Trigger
19	C2C_2	Line Trigger

2.5. LED Indicators

Applies to: Base DualBase Full FullXR

The bracket is fitted with two green LED’s mounted on a right-angled holder.

On **1623 Grablink DualBase**, the LED A is related to acquisition channel A whereas LED B is related to acquisition channel B. On **1624 Grablink Base**, **1622 Grablink Full** and **1626 Grablink Full XR**, the two LED's are related to the same acquisition channel.

LED states descriptions and possible causes

State	Description	Possible causes
OFF	The board is not working.	The board is not powered . The MultiCam driver is not loaded. The on-board FPGA is not yet configured. The board is defective.
	No Camera Link clock is received from the camera.	The camera is not connected. The camera is not powered. The camera is not initialized yet.
ON	Camera Link clock is received from the camera but both the LVAL and the FVAL signals are missing.	The camera is not initialized yet. In case of asynchronous reset camera: The frame grabber doesn't correctly deliver the Reset/Expose control signals.
	Camera Link clock is received from the camera. There is activity on LVAL or FVAL signals but the board is not acquiring data.	The MultiCam Channel is not in the READY or the ACTIVE state. The trigger conditions are not satisfied.
BLINKING	The board is acquiring data.	-

3. Electrical Specification

Electrical specification of the product(s) including: electrical characteristics of all the input/output ports, description of the power distribution, power requirements, etc.

3.1. Power Supply Requirements 48
3.2. PCI Interface 51
3.3. Camera Link Interface 54
3.4. Power over Camera Link 57
3.5. DIN* High-Speed Differential Input Ports 62
3.6. IIN* Isolated Current-Sense Input Ports 65
3.7. IOUT* Isolated Contact Output Ports 71
3.8. Power Supply Outputs 74
3.9. Chassis Ground/Signal Ground Interconnect 76

3.1. Power Supply Requirements

1624 Grablink Base

Board consumption

1624 Grablink Base draws power exclusively from both the +3.3 and +12V rails of the PCI Express connector.

Parameter	Min	Typ.	Max	Units
PCI Express +3.3V supply voltage	3.0	3.3	3.6	V
PCI Express +3.3V supply current		0.34		A
PCI Express +12V supply voltage	11.0	12	13.0	V
PCI Express +12V supply current		0.22		A
PCI Express power rail requirement		3.8	4.5	W

Notes

- The typical supply current values are measured during normal board operation at 25°C ambient temperature and nominal supply voltages.
- The maximum current on each supply rail are below the limits allowed for a 10W slot.
- The power consumption is below the 10W maximum power dissipation allowed for a low profile x1 PCI Express add-in card.

System-dependent consumption

1624 Grablink Base draws power from the "Power Input Connector" on page 43 when PoCL power is delivered to the camera or when +5V and +12V power is delivered to external loads through the System I/O connectors.

NOTE
No additional power is drawn for the PCI Express connector.

1623 Grablink DualBase

Board consumption

1623 Grablink DualBase draws power exclusively from both the +3.3 and +12V rails of the PCI Express connector.

Parameter	Min	Typ.	Max	Units
PCI Express +3.3V supply voltage	3.0	3.3	3.6	V
PCI Express +3.3V supply current		0.47		A

Parameter	Min	Typ.	Max	Units
PCI Express +12V supply voltage	11.0	12	13.0	V
PCI Express +12V supply current		0.37		A
PCI Express power rail requirement		6.0	7.2	W

Notes

- The typical supply current values are measured during normal board operation at 25°C ambient temperature and nominal supply voltages.
- The maximum current on each supply rail are below the limits allowed for a 10W slot.
- The power consumption is below the 10W maximum power dissipation allowed for a low profile x1 PCI Express add-in card.

System-dependent consumption

1623 Grablink DualBase draws power from the "Power Input Connector" on page 43 when PoCL power is delivered to the cameras or when +5V and +12V power is delivered to external loads through the System I/O connectors.

NOTE
No additional power is drawn for the PCI Express connector.

1622 Grablink Full

Board consumption

1622 Grablink Full draws power exclusively from both the +3.3 and +12V rails of the PCI Express connector.

Parameter	Min	Typ	Max	Units
PCI Express +3.3V supply voltage	3.0	3.3	3.6	V
PCI Express +3.3V supply current		0.48		A
PCI Express +12V supply voltage	11.0	12	13.0	V
PCI Express +12V supply current		0.34		A
PCI Express power rail requirement		5.7	6.9	W

Notes

- The typical supply current values are measured during normal board operation at 25°C ambient temperature and nominal supply voltages.
- The maximum current on each supply rails are below the limits allowed for a 10W slot.
- The power consumption is below the 25W maximum power dissipation allowed for a x4 PCI Express add-in card.

System-dependent consumption

1622 Grablink Full draws power from the "Power Input Connector" on page 44 when +5V and +12V power is delivered to external loads through the System I/O connectors.

NOTE
No additional power is drawn for the PCI Express connector.

1626 Grablink Full XR

Board consumption

1626 Grablink Full XR draws power exclusively from both the +3.3 and +12V rails of the PCI Express connector.

Parameter	Min	Typ	Max	Units
PCI Express +3.3V supply voltage	3.0	3.3	3.6	V
PCI Express +3.3V supply current		1.0		A
PCI Express +12V supply voltage	11.0	12	13.0	V
PCI Express +12V supply current		0.41		A
PCI Express power rail requirement		8.2	9.9	W

Notes

- The typical supply current values are measured during normal board operation at 25°C ambient temperature and nominal supply voltages.
- The maximum current on each supply rails are below the limits allowed for a 10W slot.
- The power consumption is below the 25W maximum power dissipation allowed for a x4 PCI Express add-in card.

System-dependent consumption

1626 Grablink Full XR draws power from the "Power Input Connector" on page 43 when PoCL power is delivered to the camera or when +5V and +12V power is delivered to external loads through the System I/O connectors.

NOTE
No additional power is drawn for the PCI Express connector.

3.2. PCI Interface

PCI Identification

Grablink cards are identified on the PCI bus as follows:

	Base	DualBase	Full	FullXR
PCI Vendor ID	0x1805	0x1805	0x1805	0x1805
PCI Device ID	0x030E (782)	0x030C (780)	0x030A (778)	0x0310 (784)
PCI Device ID (Recovery mode)	0x030F (783)	0x030D (781)	0x030B (779)	0x0311 (785)
PCI Sub-Vendor ID	0x0000	0x0000	0x0000	0x0000
PCI Sub-Device ID	0x0001	0x0001	0x0001	0x0001

PCI Interface Type per Product

Product	Interface Type
1624 Grablink Base	1-lane Rev 1.1 PCI Express End-point
1623 Grablink DualBase	4-lane Rev 1.1 PCI Express End-point
1622 Grablink Full	4-lane Rev 1.1 PCI Express End-point
1626 Grablink Full XR	4-lane Rev 1.1 PCI Express End-point

1-lane Rev 1.1 PCI Express End-point

Applies to: Base

The 1-lane Rev 1.1 PCI Express end-point:

- complies with revision 1.1 of the PCI Express Card Electromechanical specification,
- has a 1-lane wide connector,
- operates at 2.5 GHz,
- supports payload size up to 1024 bytes,
- supports 64-bit addressing for bus master access.

NOTE

The card can be used in any 1-lane , 4-lane or 8-lane PCIe slot. It can be also be used in a 16-lane PCIe slot that is not reserved for a graphical board.

Payload Size

During the configuration of the PCI Express fabric, the PCI Express end point interface negotiates the payload size of the TLP packets. The maximum payload size of the end point interface is 1024 bytes. The negotiated payload size is reported through the MultiCam parameter PCIePayloadSize. Possible values are 128,256, 512 and 1024.

PCIe Endpoint Interface Revision Number

The revision number of the PCI Express end point interface is reported through the MultiCam PCIeEndpointRevisionID parameter.

4-lane Rev 1.1 PCI Express End-point

Applies to: DualBase Full FullXR

The 4-lane Rev 1.1 PCI Express end-point:

- complies with revision 1.1 of the PCI Express Card Electromechanical specification,
- has a 4-lane wide connector,
- operates at 2.5 GHz,
- supports payload size up to 1024 bytes,
- supports 64-bit addressing for bus master access,
- supports 1-lane and 4-lane link widths (see table),
- allows for logical reversal of lane numbers (see table),
- offers the optimal performance when it is configured for 4-lane operation.

NOTE
The card can be used in any 1-lane , 4-lane or 8-lane PCIe slot. It can be also be used in a 16-lane PCIe slot that is not reserved for a graphical board.

Lanes Configuration

During the configuration of the PCI Express fabric, the PCI Express end point interface negotiates the link width. The negotiated link width is reported through the PCIeLinkWidth parameter. This PCI Express end point interface supports two values of link width: 1 and 4.

The width of 4 is selected when the board is plugged into a slot a having one of the two supported 4-lane configuration. In any other case, the selected width is 1.

The 4-lane PCI Express end point interface implements lane reversal, which enables the logical reversal of lane numbers.

Lane configuration	Physical lane 3	Physical lane 2	Physical lane 1	Physical lane 0
Four non-reversed lanes	Logical lane 3	Logical lane 2	Logical lane 1	Logical lane 0
Four reversed lanes starting on lane 3	Logical lane 0	Logical lane 1	Logical lane 2	Logical lane 3
One non-reversed lane				Logical lane 0
One non-reversed lane starting on lane 3	Logical lane 0			

Payload Size

During the configuration of the PCI Express fabric, the PCI Express end point interface negotiates the payload size of the TLP packets. The maximum payload size of the end point interface is 1024 bytes. The negotiated payload size is reported through the MultiCam parameter PCIePayloadSize. Possible values are 128,256, 512 and 1024.

PCIe Endpoint Interface Revision Number

The revision number of the PCI Express end point interface is reported through the MultiCam PCIeEndpointRevisionID parameter.

PCIe end-point to PC memory data transfer performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	4-lane @ 2.5 GT/s		800		MB/s

3.3. Camera Link Interface

Electrical specification of the Camera Link interface

Features Overview per product

Feature	Base	DualBase	Full	FullXR
Camera #	1	2	1	1
Channel Link #)per camera)	1	1	3	3
Clock range [MHz]	20-85	20-85	20-85 30-85*	20-85 30-85*
Configurations	Lite Base	Lite Base	Base Medium Full 80-bit	Base Medium Full 80-bit
Connector type	SDR	SDR	SDR	SDR
Interface type	ECCO	ECCO	ECCO	ECCO+
PoCL	OK	OK	-	OK

(*) Camera Link clock range is restricted to 30-85 MHz for 80-bit configurations

Abbreviations:

- *SDR:* Shrunk Delta Ribbon connector
- *ECCO:* Extended Camera Link Cable Operation; refer to About ECCO/ECCO+
- *ECCO+:* Extended Camera Link Cable Operation with equalization; refer to About ECCO/ECCO+

Channel Link

Each channel link is composed of 5 LVDS pairs:

- One LVDS pair transmits the clock to the frame grabber.
- Four LVDS pairs transmit the payload to the frame grabber at a bit rate equal to the clock frequency multiplied by 7.

Clock Line Requirements

For each channel link individually, the clock signal must satisfy the following requirements:

- Clock frequency range:

Base	DualBase	Full	FullXR
20-85	20-85	20-85 30-85*	20-85 30-85*

- The clock may not be switched off during normal operation.
- The clock jitter must be as low as possible; it is recommended to use X-Tal oscillators to generate the Camera Link clock. It may not exceed 1 ns or 20% of the clock period.
- The clock duty cycle must be better than 25%/75%.
- For correct operation of PoCL, it is mandatory to apply the clock as soon as possible after power on. The time-out delay is 500 milliseconds.

Data Lines Requirements

For each channel link individually, the electrical signal of the 4 data lines must be conform to the Camera Link requirements.

Cable Requirements

The camera cables must be Camera Link compliant and terminated with a Mini Delta Ribbon - MDR - or a Shrunk Delta Ribbon - SDR - connector :

- Connector type:

Base	DualBase	Full	FullXR
SDR	SDR	SDR	SDR

NOTE
Both PoCL and non-PoCL cables can be used.

WARNING
The usage of poor quality Camera Link cables may cause malfunction. This becomes critical for systems with a high clock rate or with long cables length. Therefore, Euresys recommends using Camera Link cables that are certified by the cable manufacturer for the length vs. clock rate combination.

Multiple Channel Links Requirements

Applies to: Full FullXR

For configurations using more than 1 channel link, it is mandatory to follow the additional requirements:

- The Camera Link standard specifies that all four enable signals are supplied to all channel links using the Medium and the Full configurations. For the 80-bit configuration, only the LVAL signal needs to be distributed on the second and the third channel link.
- In any configuration, the same LVAL signal must be applied on all channel link involved in the configuration
- At least one valid LVAL pulse needs to be sent to the frame grabber before it can start acquiring data.
- The skew across LVAL signals of all channel link receivers involved in the configuration may not exceed 2 ns (about 40 cm of cable). It is recommended to:
  - Use identical cables in terms of length and propagation delay characteristic for both connectors.
  - Apply the LVAL signal when power is on.

3.4. Power over Camera Link

Applies to: Base DualBase FullXR

PoCL Features Overview

Feature	Base	DualBase	Full	FullXR
Switchable PoCL SafePower frame grabber	OK	OK	-	OK
Single-cable PoCL Base camera #	1	2	-	1
Two-cable PoCL Medium/Full/80-bit camera #	-	-	-	1
PoCL controller #	1	2	-	2

NOTE
1623 Grablink DualBase and **1626 Grablink Full XR** are fitted with two independent PoCL controllers, one per Camera Link connector.

PoCL Controller

The PoCL controllers of Grablink cards fulfills the requirements of the Power over Camera Link (PoCL) as specified in section 4 of the Annex E of the Camera Link Standard v2.1 for Switchable PoCL SafePower frame grabbers, namely;

- SafePower Switchable power output to allow the frame grabber to operate safely with PoCL and non-POCL cameras.
- Automatic detection of PoCL cameras
- Capable of supplying up to 4W of power to the camera through each Camera Link connector
- Over-current protection (OCP)

In addition, it provides the user with:

- an AUTO/OFF control through the PoCL_Mode parameter.
- a PoCL status through the PoCL_Status parameter.

PoCL Controller Unit Specification

Parameter	Min.	Typ.	Max.	Unit
DC input voltage requirement	11	12	13	V
DC output voltage @ON-state	11	12	13	V
PoCL power output	4			W
PoCL current rating	400			mA

Power Source Requirements

The power originates from an external power source that has to be attached to the "Power Input Connector" on page 43 of **1624 Grablink Base**, **1623 Grablink DualBase** and **1626 Grablink Full XR**.

The external power source must be a regulated 12V DC power supply capable to sustain the current required by the camera(s).

NOTE
The voltage loss across the PoCL Controller Unit and its own power consumption are negligible.

NOTE
For **1623 Grablink DualBase** and **1626 Grablink Full XR**, the power source is common for both PoCL controllers.

Power Output Capabilities

A PoCL controller is capable to deliver a sustained supply current up to 400 mA to a PoCL compliant camera through a single PoCL compliant cable. Assuming a minimal supply voltage of 11 VDC and a voltage loss of 1 V in the cable, a PoCL camera can safely drawn a maximum of 4W of power through each Camera Link cable.

PoCL Operation on 1626 Grablink Full XR

Applies to: FullXR

When a PoCL Camera Link Medium, Full or 80-bit camera is attached to **1626 Grablink Full XR**, the power can be delivered through any one or both cables according to the results of the PoCL device detection performed by each PoCL controller.

Cameras that draw less than 4W may draw power from only one connector, usually the Base Camera Link connector.

Cameras that draw more than 4W must draw power from both connectors. In addition, such cameras must satisfy the following requirements:

- The camera's power supply shall be designed so that it does not draw more than 4W per cable.
- The camera's power supply shall be designed to isolate the two Camera Link connectors, i.e. power applied to one connector shall not be injected into the other one.
- The camera shall implement a voltage detection circuit that only enables the camera's power supply when power is present on both Camera Link cables.

When a PoCL Camera Link Base camera is attached to **1626 Grablink Full XR**, the power is delivered through a single cable attached on the Base Camera Link connector. Only the PoCL controller #1 is delivering power, the controller #2 remains in the "Disconnect" state.

Overcurrent Protection

Each PoCL controller embeds an overcurrent protection circuit - OCP - based upon an electronic device that controls the current delivered to the load using:

- A dV/dt limiter
- A short-circuit current limiter
- An overload current limiter
- A thermal protection

The dV/dt limiter controls the output voltage rising slope. This limits the current during the charging of the load capacitor. The short circuit current limiter is effective when a short circuit event occur. It is also effective during the charging of the load capacitor since during that phase, the load is equivalent to a short circuit.

The overload current limiter is effective when during normal operation, the load current increases excessively; when the overload level is reached, the overload current limiter will automatically reduce the current to the short circuit level.

The thermal protection limits the temperature of the electronic device by opening the circuit until the device temperature reduces sufficiently.

OCP Characteristics

Parameter	Min	Typ	Max	Units
Output voltage slew rate		0.15		V/ms
Short circuit current limit	0.6	1	1.8	A
Overload current limit	3.1	3.2	3.5	A

Overvoltage Protection

Each PoCL controller integrates an overvoltage protection circuit - OVP - that clamps the output voltage in case of a defective external power supply.

OVP characteristics

Parameter	Min	Typ	Max	Units
Output clamping voltage	13	15	17	V

PoCL Device Detector

Each PoCL controller implements a PoCL device detector that measures the input impedance of the camera power input circuit at the off state and check if it is within the specified limits specified for PoCL camera Link cameras.

Therefore, a calibrated sense current is injected by the frame grabber into the power input circuit of the camera through the camera cable. After the expiration of the "sense time delay" time interval that allows the input capacitance to be charged, the detector measures repetitively the voltage during the "Sense OK time". If the voltage stays between the thresholds, the power is applied.

The camera must deliver a clock within the "initial clock turn-on delay" after the application of the power. If this is not the case, the frame grabber turns off the power immediately.

While the camera is powered, the PoCL device detector monitors continuously the Camera Link clock. If this clock is interrupted during at least "turn-off delay after clock loss" time interval, the power is immediately turned off.

PoCL device detector characteristics

Parameter	Min	Typ	Max	Units
Sense current on 10K impedance load	30	52	75	µA
Detector thresholds	0.3		1.2	V
Allowable impedance range	8	10	12	kΩ
PoCL camera detector sense time delay		500		ms
PoCL camera detector sense OK time		500		ms
Initial clock turn-on delay		500		ms
Turn-off delay after clock-loss		500		ms

PoCL Cable Requirements

Current Capacity for PoCL Cables

Camera Link Standard (version 2.0) requires that the power and drain wires within a cable assembly shall be capable of handling 1.0 A camera current under fault conditions. The power and drain wires shall be at least AWG 28 or larger diameter.

Conductor Resistance for PoCL Cables

Camera Link Standard (version 2.0) requires that the DC resistance of any power wire or drain wire shall not exceed 2.5 Ω for the length of the cable assembly.

NOTE
The overall voltage drop on the loop is 1.0V ensuring at least 10V at the camera side for the minimal supply voltage of 11 V.

Considering that AWG 28 conductors have a typical resistance per unit length of 0,21 Ω/meter, cables using this wire gauge satisfy the above requirements for cable lengths up to 11 meters.

NOTE
The 10V minimal voltage requirement at the camera side can be satisfied with longer cables if the minimal supply voltage is higher than 11 V or if the camera draws less than 400 mA.

Disabling PoCL Automatic Activation

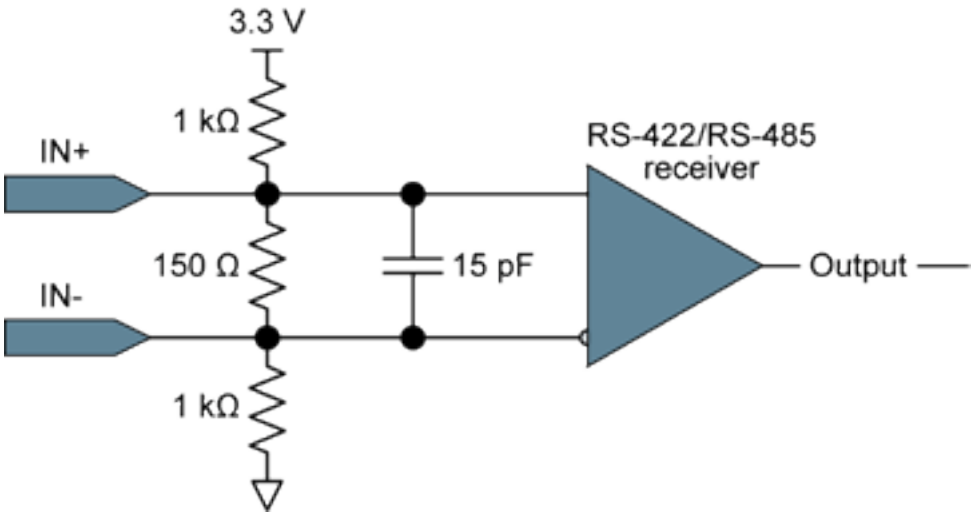
To avoids unexpected activation of PoCL when the camera is not powered trough the Camera Link cable:

1. Before Channel activation: set PoCL_Mode to OFF
2. Set ChannelState to READY

3.5. DIN* High-Speed Differential Input Ports

Applies to: Base DualBase Full FullXR

Characteristics



High-speed differential inputs (simplified schematic)

The high-speed differential input ports have the following characteristics:

Non-isolated ANSI/TIA/EIA-422-B differential line receiver

- -7V / +12V common mode
- 4 kV contact, 8 kV air discharge ESD protection
- Minimum pulse width: 100 nanoseconds (or better)
- Maximum 10%-90% rise/fall time: 1 µs
- Maximum pulse rate: up to 5 MHz
- Fixed termination (not removable)
- Guaranteed 'High' input state when unconnected (hardware failsafe circuit)
- HF noise filtering

The state of the port is reported through the InputState MultiCam parameter.

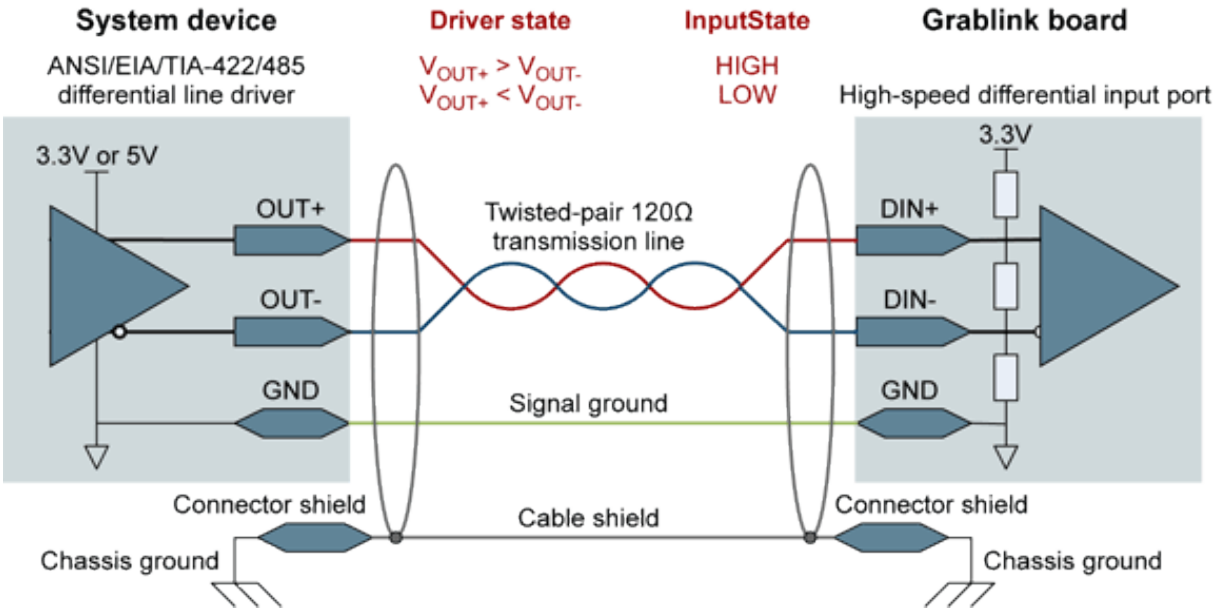
Compatible Drivers

The following drivers are compatible with the high-speed differential input ports:

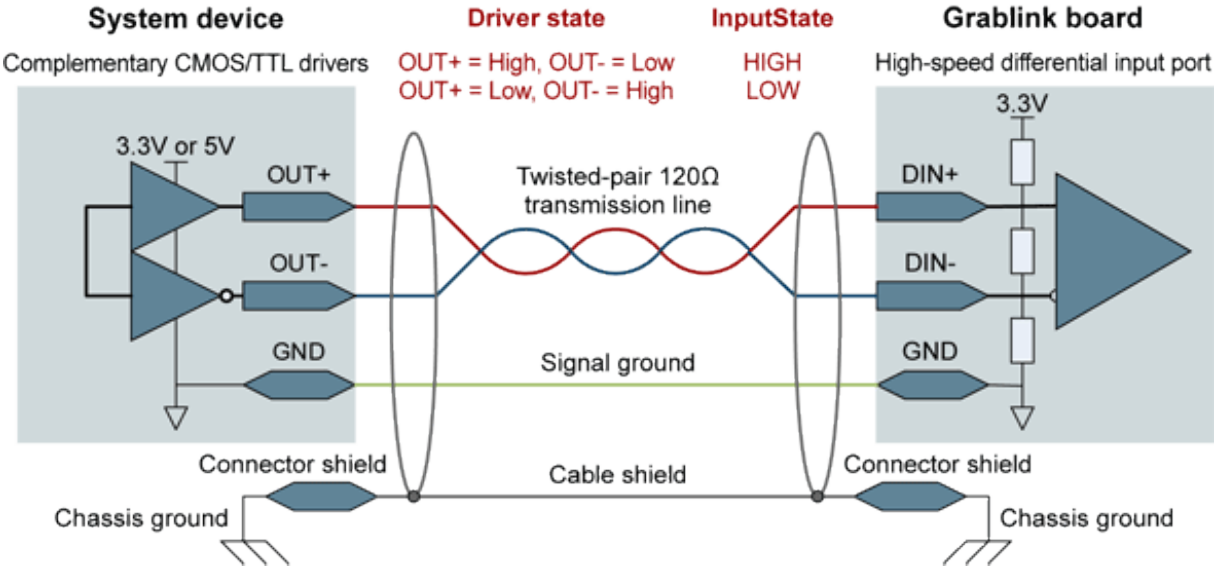
- ANSI/EIA/TIA-422/485 differential line drivers
- Complementary TTL drivers

Electrical Circuits Examples

The following figure shows the recommended wiring diagram for a system device using RS-422 differential drivers. Applicable for fast system devices such as motion encoders operating at frequencies up to 5 MHz



The following figure shows the recommended wiring diagram for a system device using two complementary CMOS or TTL drivers. Applicable for fast system devices such as motion encoders operating at frequencies up to 5 MHz



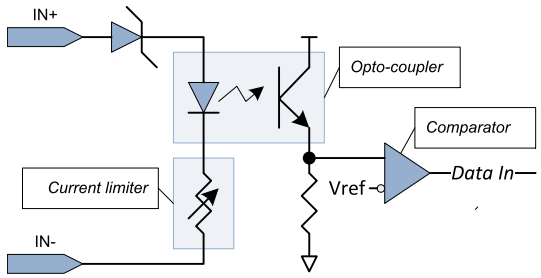
NOTE

For correct operation of the above two circuits, it is mandatory to satisfy the common-mode voltage requirements of the receiver. Practically, this requirement can be achieved by the addition of one "Signal Ground" wire between each system device and the board.

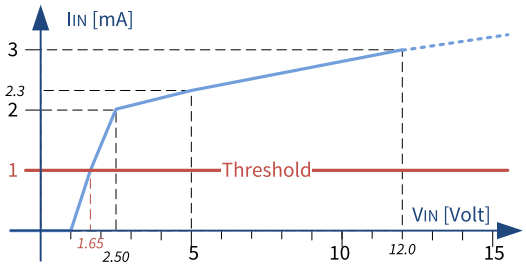
3.6. IIN* Isolated Current-Sense Input Ports

Applies to: Base DualBase Full FullXR

Isolated current-sense input with wide voltage input range up to 30V, compatible with totem-pole LVTTL, TTL, 5V CMOS drivers, RS-422 differential line drivers, potential free contacts, solid-state relays and opto-couplers



Simplified schematic



Input Current vs. Input Voltage Characteristics

DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential voltage		-30		+30	V
Input current threshold			1		mA
Differential voltage	@1 mA	1.5	1.65	1.9	V
Input current	@(VIN+ - VIN-) < 1 V			10	µA
	@(VIN+ - VIN-) = 1.65 V		1		mA
	@(VIN+ - VIN-) = 2.5 V		2		mA
	@(VIN+ - VIN-) = 5 V		2.3		mA
	@(VIN+ - VIN-) = 12 V		3		mA
	@(VIN+ - VIN-) = 30 V			5	mA

AC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Positive pulse width		10			µs
Negative pulse width		10			µs
Pulse rate		0		50	kHz
Turn-ON delay[1]	30°C; 50 kHz; 2 V square wave signal ***TrigFilter= ON (Filter delay = 500 ns)		2.1		µs
Turn-OFF delay[2]			4.5		µs

NOTE

1. The "Turn-ON" delay is defined as the time difference between a transition of state at the input that turns ON the opto-coupler and the subsequent transition in the FPGA.
2. The "Turn-OFF" delay is defined as the time difference between a transition of state at the input that turns OFF the opto-coupler and the subsequent transition in the FPGA.

These delays include the delay introduced by the digital line filter controlled by the TrigFilter, LineTrigFilter or EndTrigFilter MultiCam parameters!

Isolation characteristics

Parameter	Value
Isolation grade	Functional
Max. DC voltage	250 V
Max. AC voltage	170 V_{RMS}

NOTE

The functional isolation is only for the circuit technical protection. It does not provide an isolation that can protect a human being from electrical shock!

Logical map

The state of the port is reported as follows:

Input current	Logical State
I_{IN} > 1 mA	HIGH
I_{IN} < 1 mA	LOW
Unconnected input port	LOW

Compatible drivers

The following drivers are compatible with this version of the isolated current-sense inputs:

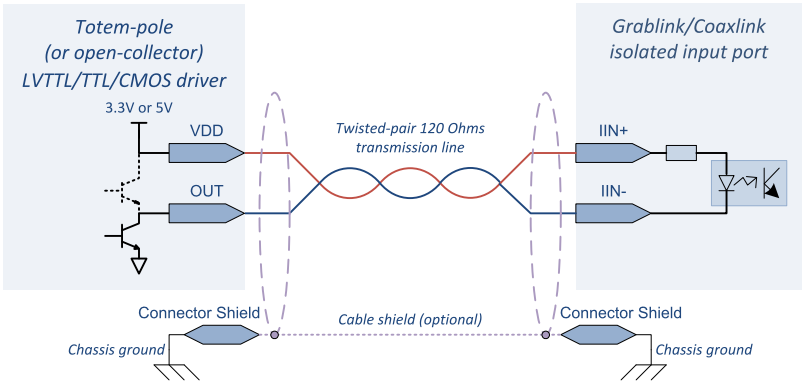
- Totem-pole LVTTL, TTL, 5 V CMOS drivers
- RS-422 Differential line drivers
- Potential free contact, solid-state relay, or opto-isolators
- 12 V and 24 V signaling voltages are also accepted

NOTE

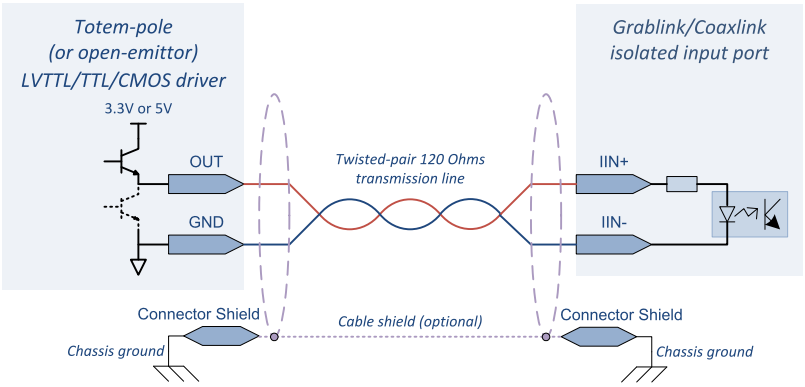
- The +12 V power supply on the I/O connector(s) can be used for powering drivers requiring a power supply.
- No external resistors are required. However, to obtain the best noise immunity with 12 V and 24 V signaling, it is recommended to insert a series resistor in the circuit. The recommended resistor values are: 4.7k Ohms for 12 V signaling and 10k Ohms for 24 V signaling.

Electrical circuit examples for 3V3 or 5V logic drivers

The following figure shows the wiring diagram for a system device using totem-pole (or open-collector) 3.3V low-voltage TTL, 5V TTL, or 5V CMOS drivers. With this circuit diagram, the highest transistor of the totem-pole driver is useless.

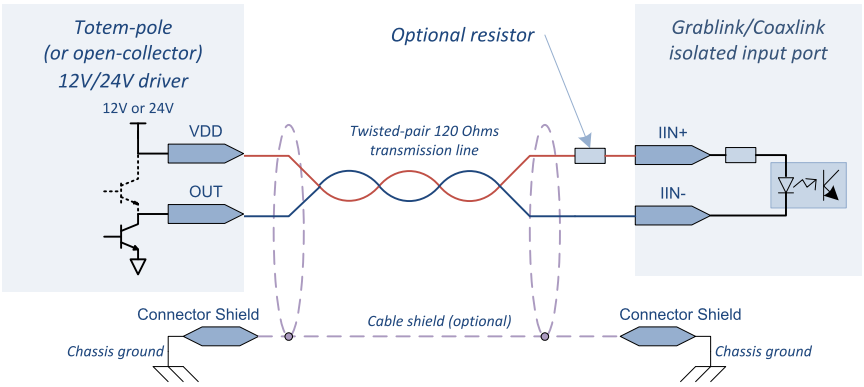


The following figure shows the wiring diagram for a system device using totem-pole (or open-emittor) 3.3V low-voltage TTL, 5V TTL, or 5V CMOS drivers. With this circuit diagram, the lowest transistor of the totem-pole driver is useless.

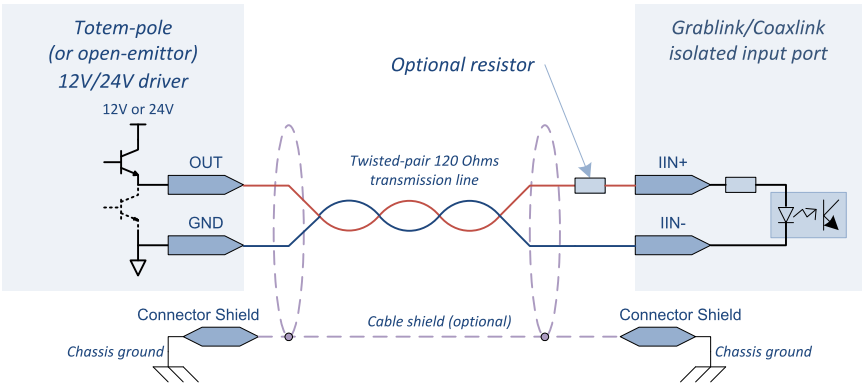


Electrical circuit examples for 12V or 24V logic drivers

The following figure shows the wiring diagram for a system device using totem-pole (or open-collector) 12V, or 24V CMOS drivers. With this circuit diagram, the highest transistor of the totem-pole driver is useless.



The following figure shows the wiring diagram for a system device using totem-pole (or open-emittor) 12V, or 24V CMOS drivers. With this circuit diagram, the lowest transistor of the totem-pole driver is useless.



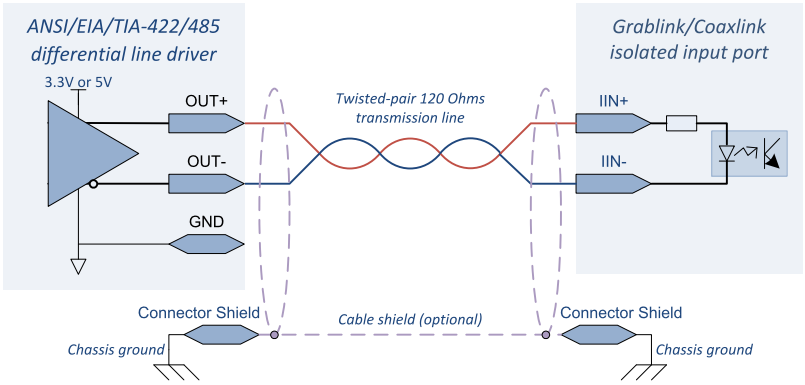
Notes

For the two above circuits:

- Operation without series resistor is allowed due to the current limiting function of the input ports.
- Better noise immunity is obtained by inserting a series resistor in the circuit. The recommended resistor values are: 4.7 kΩ for 12V signaling and 10 kΩ for 24V signaling.

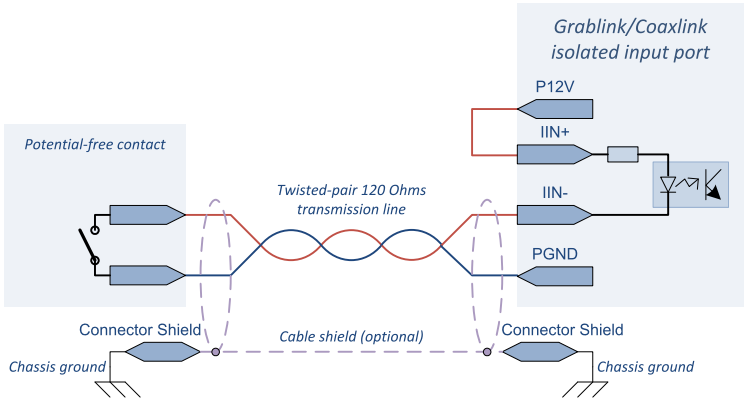
Electrical circuit example for RS-422 differential logic drivers

The following figure shows an alternate wiring diagram for a system device using RS-422 differential drivers. This alternate solution has to be used when no more high-speed differential input ports are available and when the pulse width of the transmitted signals exceeds or equal 5 microseconds.



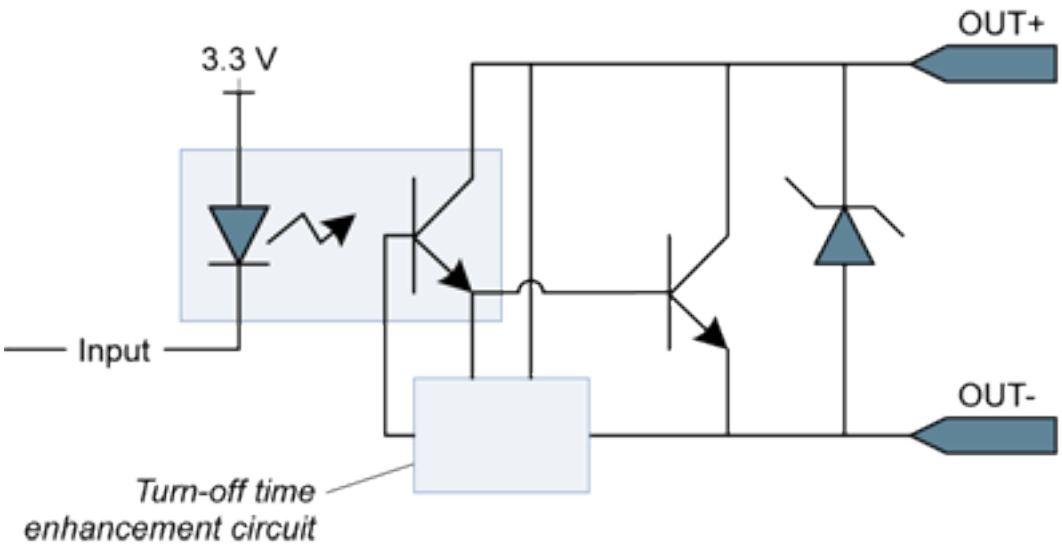
Electrical circuit example for potential-free contact

The following figure shows the wiring diagram for a system device using potential-free contacts. In this circuit, the current is supplied by the board.



3.7. IOUT* Isolated Contact Output Ports

Applies to: Base DualBase Full FullXR



Isolated contact output (simplified schematic)

The output port implements an isolated contact output.

DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Current				100	mA
Differential voltage	Open state	-30		30	V
	Closed state @ 1 mA			0.4	V
	Closed state @ 100 mA			1.0	V

NOTE

- The output port in the closed state has no current limiter, the user circuit must be designed to avoid excessive currents that could destroy the output port.
- The output port remains in the OFF-state until it is under control of the application.

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse rate	0		100	kHz
Turn-on time			5	µs
Turn-off time			5	µs

Typical switching performance @ 25°C

Current [mA]	Turn ON time [µs]	Turn OFF time [µs]
0.5	2.0	4.8
1.0	2.0	3.9
4.0	2.2	3.3
10	2.3	2.7
40	2.3	2.7
100	2.3	2.7

Isolation characteristics

Parameter	Value
Isolation grade	Functional
Max. DC voltage	250 V
Max. AC voltage	170 V_{RMS}

NOTE
The functional isolation is only for the circuit technical protection. It does not provide an isolation that can protect a human being from electrical shock!

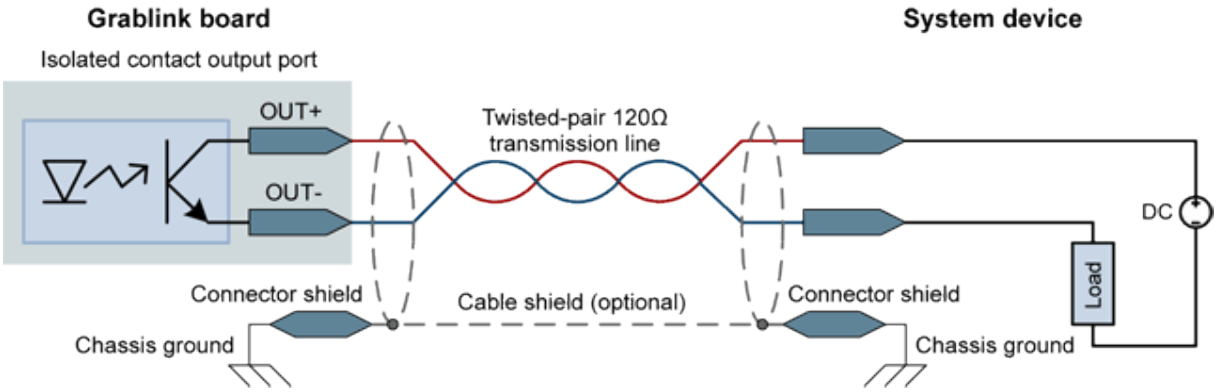
Compatible loads

The following loads are compatible with the isolated contact output ports:

- Any load within the 30 V / 100 mA envelope is accepted. The power originates from an external power source or alternatively from the power delivered through the 12 V and GND pins of the I/O connectors.

Electrical Circuits Examples

In this circuit, the current is supplied by the system device.



Notes

- The isolated output is polarized.
- In case of polarity reversal, the output port acts as a closed contact.
- The isolated output is capable to deliver up to 100 mA and to switch voltages up to 30 V.
- Exceeding 100 mA or 30V may damage the output port.
- The +5V/+12V power may be delivered by the board.

3.8. Power Supply Outputs

Applies to: Base DualBase Full FullXR

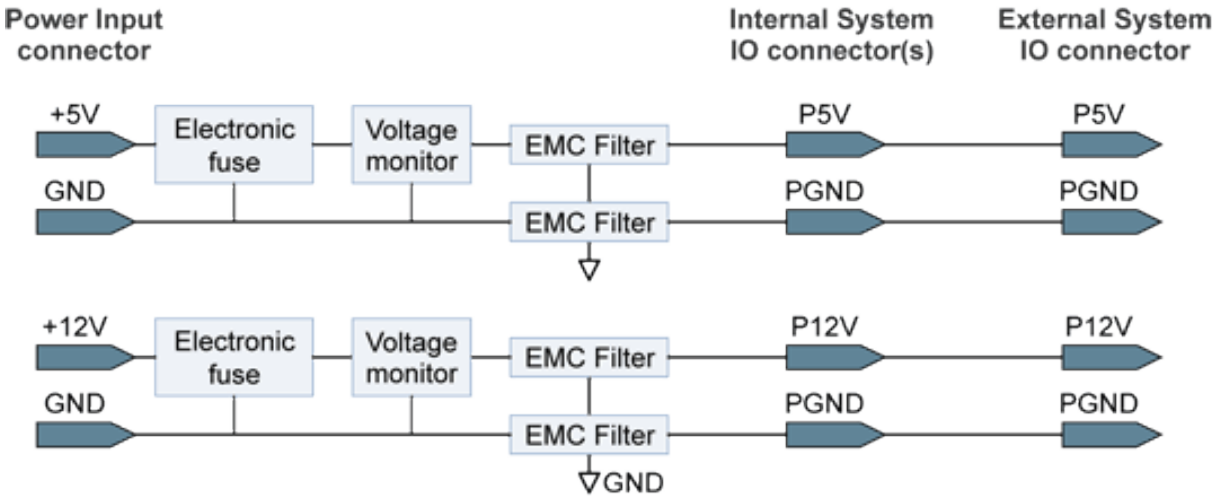
Specification of the power outputs of the I/O connectors

Non-isolated +5V and +12V power outputs are available on every I/O connectors.

Power output specification

Parameter	Conditions	Min.	Typ.	Max.	Units
Aggregated +5V output current	Operating temperature range			1.0	A
Aggregated +12V output current	Operating temperature range			1.0	A
Voltage drop across the electronic fuse	Max. output current			0.2	V

NOTE
The above specification applies over the whole operating temperature range of the Grablink card.



Power supply output

The power originates from external +5V and +12V supplies attached to the "Power Input Connector" on page 43.

NOTE
It is mandatory to connect a hard disk power supply cable to the power input connector if an application requires one or both of these power outputs.

Each power input line is fitted with an electronic fuse and a voltage monitor.

The electronic fuse provides the following protections:

- Limits the inrush current during power on sequence
- Protects the Grablink card and the power source against overload
- Protects the Grablink card and the power source against short-circuits.

WARNING
The sum of the load currents drawn from the 5V outputs of the I/O connectors must be lower or equal to 1.0 A over the whole operating temperature range of the board.

WARNING
The sum of the load currents drawn from the 12V outputs of the I/O connectors must be lower or equal to 1.0 A over the whole operating temperature range of the board.

The voltage monitors continuously compare the +5V and +12V voltage against following thresholds:

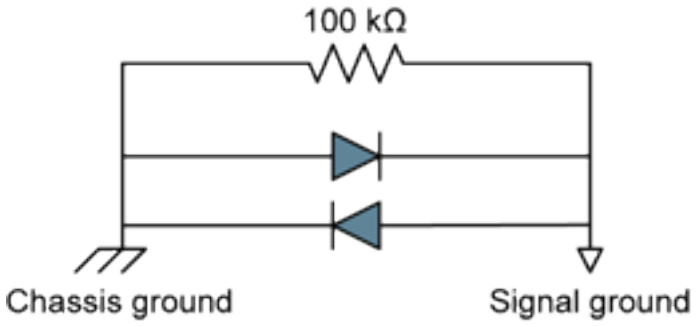
Characteristics	Min.	Typ.	Max.	Units
+5V voltage monitor threshold	0.9	3.1	4.4	V
+12V voltage monitor threshold	4.2	7.3	10.4	V

and reports the result as logical state of POWERSTATE5V and **POWERSTATE12V** input lines.

Result	State
Below threshold	LOW
Above threshold	HIGH

3.9. Chassis Ground/Signal Ground Interconnect

Applies to: Base DualBase Full FullXR



Chassis ground / Signal ground interconnect

The "Chassis ground" electrical net is connected to the "Signal ground" electrical net through a network as shown in the figure above. This prevents against significant voltages to be developed between the two nets.

Together with the cable shield and resistor, it provides an additional path for the (DC) return current of the camera power supply.

Notes

- The "Chassis ground" net includes, the metallic bracket and the metallic shell of the connectors mounted on the bracket.
- The "Signal ground" net is actually the reference potential for all the on-board electric circuits.
- It is mandatory to firmly attach the bracket on the chassis by means of the screw. This establishes a good electrical path between the card bracket and the chassis of the PC and hence avoids excessive current into the diodes.

4. Environmental Specification

Environmental specification of the product(s) including: climatic requirements, electromagnetic standards compliance statements, safety standards compliance statements, etc.

4.1. Environmental Conditions 78
4.2. Compliance Statements 79

4.1. Environmental Conditions

Storage and operating conditions specification of standard climatic class products

Storage Conditions

Parameter	Conditions	Min	Max	Units
Ambient air temperature		-20 [-4]	70 [158]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

Operating Conditions

Parameter	Conditions	Min	Max	Units
Ambient air temperature*		0 [32]	50 [122]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

(*) The ambient air temperature is measured in the close vicinity of the heatsink, at a distance of about 10 mm above the printed circuit board.

4.2. Compliance Statements

Environmental regulations compliance statements

CE/UKCA Compliance Statement

CE	**Notice for Europe** This product is in conformity with the Council Directive 2014/30/EU
UK CA	**Notice for Great Britain** This product is in conformity with Electromagnetic Compatibility Regulations 2016

This piece of equipment has been tested and found to comply with Class B EN55022/CISPR22 electromagnetic emission requirements and EN55024/CISPR24 electromagnetic susceptibility.

This product has been tested in typical class A and class B compliant host systems. It is assumed that this product will also achieve compliance in any class A or class B compliant unit.

To meet EC and Great Britain requirements, shielded cables must be used to connect a peripheral to the card.

FCC Compliance Statement

FC	**Notice for USA** Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation or when the equipment is operated in a commercial environment.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

KC Compliance Statement

Notice for Korea
The following products have been registered under the Clause 3, Article 58-2 of Radio Wave Acts:

Product	KC Registration Number
1623 Grablink DualBase	MSIP-REM-EUr-PC1623
1626 Grablink Full XR	MSIP-REM-EUr-PC1626
1622 Grablink Full	MSIP-REM-EUr-PC1622
1624 Grablink Base	MSIP-REM-EUr-PC1624

RoHS Compliance Statement

This product is in conformity with the European Union RoHS 2015/863 (ROHS3) Directive, that stands for "the restriction of the use of certain hazardous substances in electrical and electronic equipment".

WEEE Statement

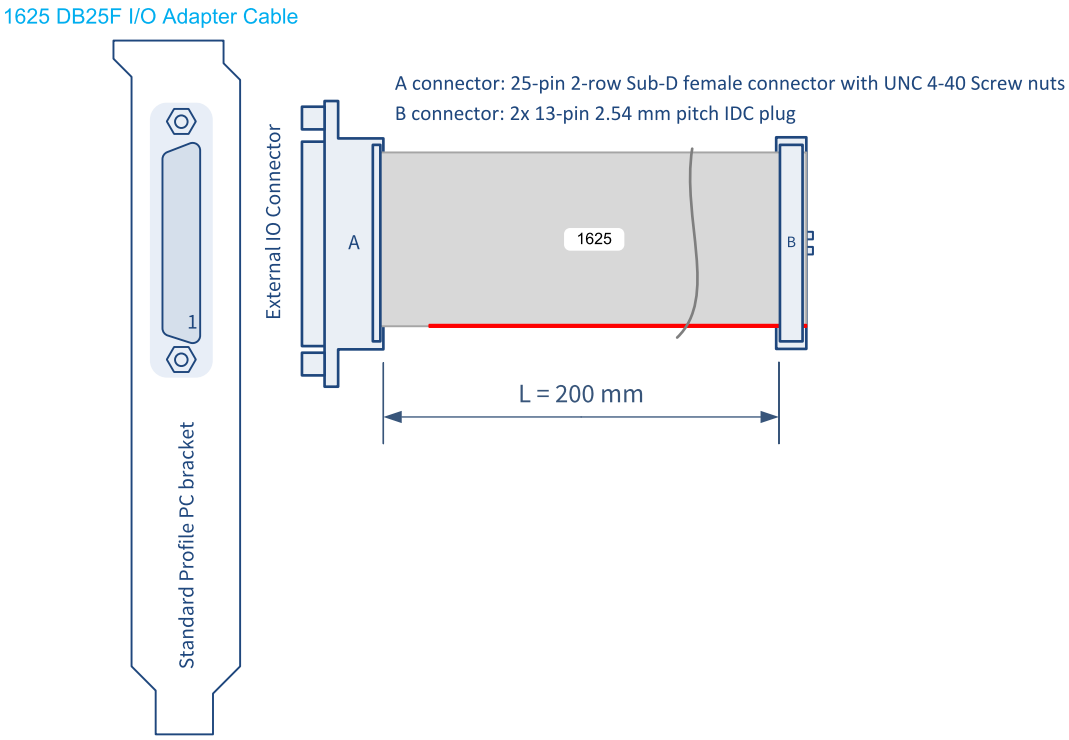
According the European directive 2012/19/EU, the product must be disposed of separately from normal household waste. It must be recycled according to the local regulations.

5. Related Products & Accessories

5.1. 1625 DB25F I/O Adapter Cable 82
5.2. 3304 HD26F I/O Adapter Cable 86
5.3. 3305 C2C SyncBus cable 90
5.4. 3306 C2C Quad SyncBus Cable 91
5.5. Camera Link Cables 92

5.1. 1625 DB25F I/O Adapter Cable

Applies to: DualBase Full FullXR



The **1625 DB25F I/O Adapter Cable** connects all the pins (but the pin 1) of a 26-pin dual-row 0.1" pitch connector to a 25-pin female SubD connector fitted into a standard-profile PC bracket.

Usage with "Internal I/O Connector" on page 37

Applies to: Full FullXR

The adapter brings the set of I/O lines and the +5V/+12V power outputs to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1		GND	Ground
2	2	1	GND	Ground
3	3	14	DIN1+	High-speed differential input #1 – Positive pole
4	4	2	DIN1-	High-speed differential input #1 – Negative pole
5	5	15	DIN2+	High-speed differential input #2 – Positive pole

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
6	6	3	DIN2-	High-speed differential input #2 – Negative pole
7	7	16	IIN1+	Isolated input #1 – Positive pole
8	8	4	IIN1-	Isolated input #1 – Negative pole
9	9	17	IIN2+	Isolated input #2 – Positive pole
10	10	5	IIN2-	Isolated input #2 – Negative pole
11	11	18	IIN3+	Isolated input #3 – Positive pole
12	12	6	IIN3-	Isolated input #3 – Negative pole
13	13	19	IIN4+	Isolated input #4 – Positive pole
14	14	7	IIN4-	Isolated input #4 – Negative pole
15	15	20	IOUT1+	Isolated contact output #1 – Positive pole
16	16	8	IOUT1-	Isolated contact output #1 – Negative pole
17	17	21	IOUT2+	Isolated contact output #2 – Positive pole
18	18	9	IOUT2-	Isolated contact output #2 – Negative pole
19	19	22	IOUT3+	Isolated contact output #3 – Positive pole
20	20	10	IOUT3-	Isolated contact output #3 – Negative pole
21	21	23	IOUT4+	Isolated contact output #4 – Positive pole
22	22	11	IOUT4-	Isolated contact output #4 – Negative pole
23	23	24	+5V	+5 V Power output
24	24	12	GND	Ground
25	25	25	+12V	+12 V Power output
26	26	13	+12V_RTN	Ground

Usage with "Channel A Internal I/O Connector" on page 39

Applies to: DualBase

The adapter brings the first set of I/O lines and the +5V/+12V power outputs to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1		GND	Ground
2	2	1	GND	Ground
3	3	14	DIN1A+	Channel A - High-speed differential input #1 – Positive pole
4	4	2	DIN1A-	Channel A - High-speed differential input #1 – Negative pole

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
5	5	15	DIN2A+	Channel A - High-speed differential input #2 – Positive pole
6	6	3	DIN2A-	Channel A - High-speed differential input #2 – Negative pole
7	7	16	IIN1A+	Channel A - Isolated input #1 – Positive pole
8	8	4	IIN1A-	Channel A - Isolated input #1 – Negative pole
9	9	17	IIN2A+	Channel A - Isolated input #2 – Positive pole
10	10	5	IIN2A-	Channel A - Isolated input #2 – Negative pole
11	11	18	IIN3A+	Channel A - Isolated input #3 – Positive pole
12	12	6	IIN3A-	Channel A - Isolated input #3 – Negative pole
13	13	19	IIN4A+	Channel A - Isolated input #4 – Positive pole
14	14	7	IIN4A-	Channel A - Isolated input #4 – Negative pole
15	15	20	IOUT1A+	Channel A - Isolated contact output #1 – Positive pole
16	16	8	IOUT1A-	Channel A - Isolated contact output #1 – Negative pole
17	17	21	IOUT2A+	Channel A - Isolated contact output #2 – Positive pole
18	18	9	IOUT2A-	Channel A - Isolated contact output #2 – Negative pole
19	19	22	IOUT3A+	Channel A - Isolated contact output #3 – Positive pole
20	20	10	IOUT3A-	Channel A - Isolated contact output #3 – Negative pole
21	21	23	IOUT4A+	Channel A - Isolated contact output #4 – Positive pole
22	22	11	IOUT4A-	Channel A - Isolated contact output #4 – Negative pole
23	23	24	+5V	+5 V Power output
24	24	12	GND	Ground
25	25	25	+12V	+12 V Power output
26	26	13	+12V_RTN	Ground

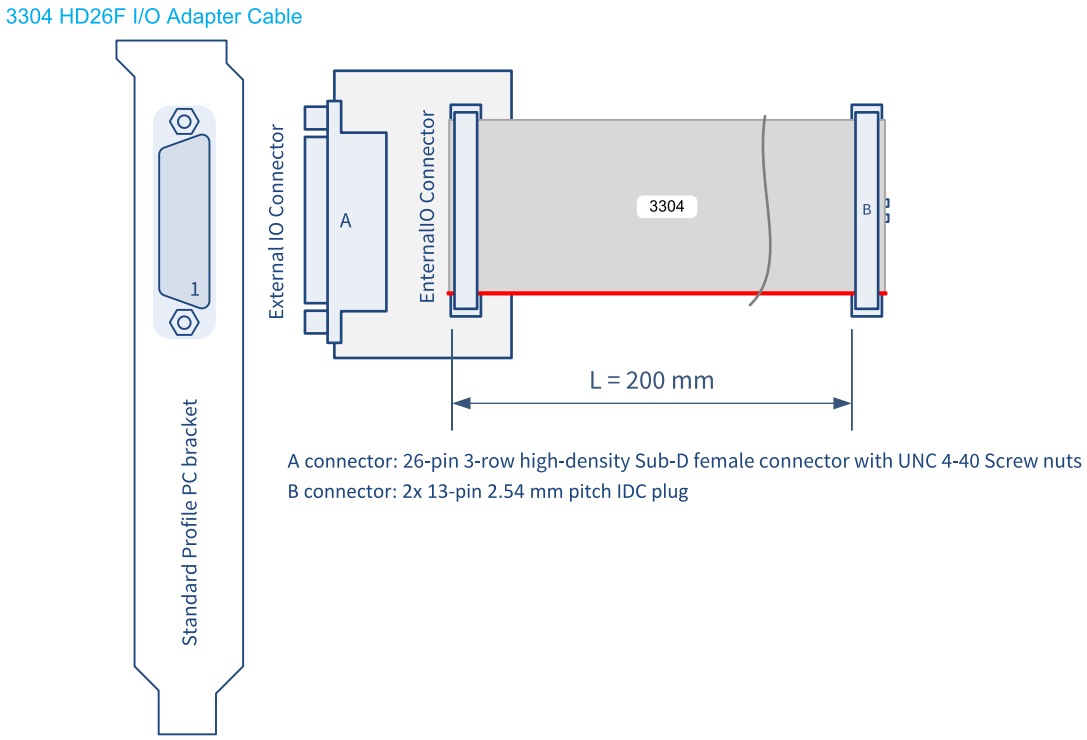
Usage with "Channel B Internal I/O Connector" on page 41

Applies to: DualBase

The adapter brings the second set of I/O lines and the +5V/+12V power outputs to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1		GND	Ground
2	2	1	GND	Ground
3	3	14	DIN1B+	Channel B - High-speed differential input #1 – Positive pole
4	4	2	DIN1B-	Channel B - High-speed differential input #1 – Negative pole
5	5	15	DIN2B+	Channel B - High-speed differential input #2 – Positive pole
6	6	3	DIN2B-	Channel B - High-speed differential input #2 – Negative pole
7	7	16	IIN1B+	Channel B - Isolated input #1 – Positive pole
8	8	4	IIN1B-	Channel B - Isolated input #1 – Negative pole
9	9	17	IIN2B+	Channel B - Isolated input #2 – Positive pole
10	10	5	IIN2B-	Channel B - Isolated input #2 – Negative pole
11	11	18	IIN3B+	Channel B - Isolated input #3 – Positive pole
12	12	6	IIN3B-	Channel B - Isolated input #3 – Negative pole
13	13	19	IIN4B+	Channel B - Isolated input #4 – Positive pole
14	14	7	IIN4B-	Channel B - Isolated input #4 – Negative pole
15	15	20	IOUT1B+	Channel B - Isolated contact output #1 – Positive pole
16	16	8	IOUT1B-	Channel B - Isolated contact output #1 – Negative pole
17	17	21	IOUT2B+	Channel B - Isolated contact output #2 – Positive pole
18	18	9	IOUT2B-	Channel B - Isolated contact output #2 – Negative pole
19	19	22	IOUT3B+	Channel B - Isolated contact output #3 – Positive pole
20	20	10	IOUT3B-	Channel B - Isolated contact output #3 – Negative pole
21	21	23	IOUT4B+	Channel B - Isolated contact output #4 – Positive pole
22	22	11	IOUT4B-	Channel B - Isolated contact output #4 – Negative pole
23	23	24	+5V	+5 V Power output
24	24	12	GND	Ground
25	25	25	+12V	+12 V Power output
26	26	13	+12V_RTN	Ground

5.2. 3304 HD26F I/O Adapter Cable



The **3304 HD26F I/O Adapter Cable** interconnects a 26-pin dual-row 0.1" pitch connector to a 26-pin 3-row female High-density SubD connector fitted into a standard-profile PC bracket.

Usage with "Internal I/O Connector" on page 37

Applies to: Full FullXR

The adapter brings the set of I/O lines and the +5V/+12V power outputs to a bracket-mount High-density SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1	1	GND	Ground
2	2	10	GND	Ground
3	3	20	DIN1+	High-speed differential input #1 – Positive pole
4	4	19	DIN1-	High-speed differential input #1 – Negative pole
5	5	13	DIN2+	High-speed differential input #2 – Positive pole
6	6	11	DIN2-	High-speed differential input #2 – Negative pole
7	7	3	IIN1+	Isolated input #1 – Positive pole
8	8	12	IIN1-	Isolated input #1 – Negative pole

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
9	9	13	IIN2+	Isolated input #2 – Positive pole
10	10	21	IIN2-	Isolated input #2 – Negative pole
11	11	14	IIN3+	Isolated input #3 – Positive pole
12	12	4	IIN3-	Isolated input #3 – Negative pole
13	13	15	IIN4+	Isolated input #4 – Positive pole
14	14	5	IIN4-	Isolated input #4 – Negative pole
15	15	23	IOUT1+	Isolated contact output #1 – Positive pole
16	16	22	IOUT1-	Isolated contact output #1 – Negative pole
17	17	16	IOUT2+	Isolated contact output #2 – Positive pole
18	18	6	IOUT2-	Isolated contact output #2 – Negative pole
19	19	25	IOUT3+	Isolated contact output #3 – Positive pole
20	20	24	IOUT3-	Isolated contact output #3 – Negative pole
21	21	17	IOUT4+	Isolated contact output #4 – Positive pole
22	22	7	IOUT4-	Isolated contact output #4 – Negative pole
23	23	8	+5V	+5 V Power output
24	24	9	GND	Ground
25	25	26	+12V	+12 V Power output
26	26	18	+12V_RTN	Ground

Usage with "Channel A Internal I/O Connector" on page 39

Applies to: DualBase

The adapter brings the first set of I/O lines and the +5V/+12V power outputs to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1	1	GND	Ground
2	2	10	GND	Ground
3	3	20	DIN1A+	Channel A - High-speed differential input #1 – Positive pole
4	4	19	DIN1A-	Channel A - High-speed differential input #1 – Negative pole
5	5	13	DIN2A+	Channel A - High-speed differential input #2 – Positive pole
6	6	11	DIN2A-	Channel A - High-speed differential input #2 – Negative pole
7	7	3	IIN1A+	Channel A - Isolated input #1 – Positive pole

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
8	8	12	IIN1A-	Channel A - Isolated input #1 – Negative pole
9	9	13	IIN2A+	Channel A - Isolated input #2 – Positive pole
10	10	21	IIN2A-	Channel A - Isolated input #2 – Negative pole
11	11	14	IIN3A+	Channel A - Isolated input #3 – Positive pole
12	12	4	IIN3A-	Channel A - Isolated input #3 – Negative pole
13	13	15	IIN4A+	Channel A - Isolated input #4 – Positive pole
14	14	5	IIN4A-	Channel A - Isolated input #4 – Negative pole
15	15	23	IOUT1A+	Channel A - Isolated contact output #1 – Positive pole
16	16	22	IOUT1A-	Channel A - Isolated contact output #1 – Negative pole
17	17	16	IOUT2A+	Channel A - Isolated contact output #2 – Positive pole
18	18	6	IOUT2A-	Channel A - Isolated contact output #2 – Negative pole
19	19	25	IOUT3A+	Channel A - Isolated contact output #3 – Positive pole
20	20	24	IOUT3A-	Channel A - Isolated contact output #3 – Negative pole
21	21	17	IOUT4A+	Channel A - Isolated contact output #4 – Positive pole
22	22	7	IOUT4A-	Channel A - Isolated contact output #4 – Negative pole
23	23	8	+5V	+5 V Power output
24	24	9	GND	Ground
25	25	26	+12V	+12 V Power output
26	26	18	+12V_RTN	Ground

Usage with "Channel B Internal I/O Connector" on page 41

Applies to: DualBase

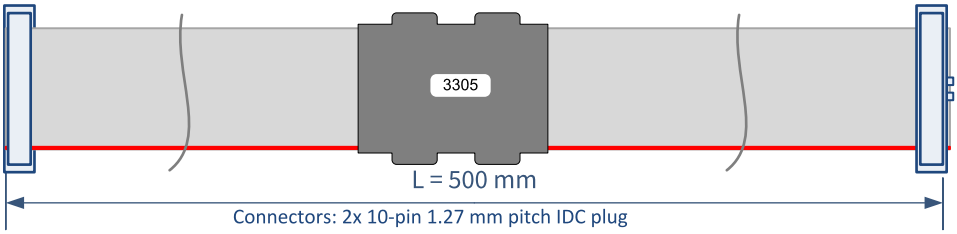
The adapter brings the second set of I/O lines and the +5V/+12V power outputs to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1	1	GND	Ground
2	2	10	GND	Ground
3	3	20	DIN1B+	Channel B - High-speed differential input #1 – Positive pole
4	4	19	DIN1B-	Channel B - High-speed differential input #1 – Negative pole
5	5	13	DIN2B+	Channel B - High-speed differential input #2 – Positive pole
6	6	11	DIN2B-	Channel B - High-speed differential input #2 – Negative pole

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
7	7	3	IIN1B+	Channel B - Isolated input #1 – Positive pole
8	8	12	IIN1B-	Channel B - Isolated input #1 – Negative pole
9	9	13	IIN2B+	Channel B - Isolated input #2 – Positive pole
10	10	21	IIN2B-	Channel B - Isolated input #2 – Negative pole
11	11	14	IIN3B+	Channel B - Isolated input #3 – Positive pole
12	12	4	IIN3B-	Channel B - Isolated input #3 – Negative pole
13	13	15	IIN4B+	Channel B - Isolated input #4 – Positive pole
14	14	5	IIN4B-	Channel B - Isolated input #4 – Negative pole
15	15	23	IOUT1B+	Channel B - Isolated contact output #1 – Positive pole
16	16	22	IOUT1B-	Channel B - Isolated contact output #1 – Negative pole
17	17	16	IOUT2B+	Channel B - Isolated contact output #2 – Positive pole
18	18	6	IOUT2B-	Channel B - Isolated contact output #2 – Negative pole
19	19	25	IOUT3B+	Channel B - Isolated contact output #3 – Positive pole
20	20	24	IOUT3B-	Channel B - Isolated contact output #3 – Negative pole
21	21	17	IOUT4B+	Channel B - Isolated contact output #4 – Positive pole
22	22	7	IOUT4B-	Channel B - Isolated contact output #4 – Negative pole
23	23	8	+5V	+5 V Power output
24	24	9	GND	Ground
25	25	26	+12V	+12 V Power output
26	26	18	+12V_RTN	Ground

5.3. 3305 C2C SyncBus cable

Applies to: Full FullXR



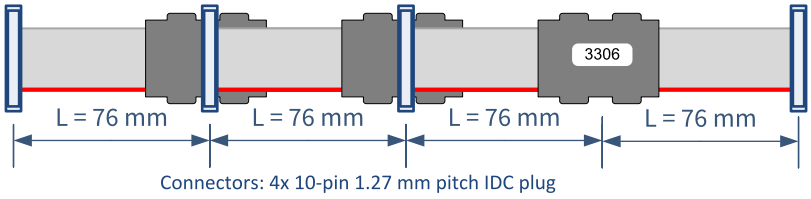
3305 C2C SyncBus cable

The **3305 C2C SyncBus cable** interconnects the "C2C SyncBus Connector" on page 45 of 2 **Grablink Full** or **Grablink Full XR** cards located in the same PC.

It enables the synchronization of 2 cameras .

5.4. 3306 C2C Quad SyncBus Cable

Applies to: Full FullXR



3306 C2C SyncBus cable

The **3306 C2C SyncBus** cable interconnects the "C2C SyncBus Connector" on page 45 of up to 4 **Grablink Full** or **Grablink Full XR** located in the same PC.

It enables the synchronization of up to 4 cameras .

5.5. Camera Link Cables

Universal Camera Link Cable

Cable Connectors

Designator	Connector family	Description
MDR	Mini Delta Ribbon	1.27 mm-pitch blade 26-blade 2-row male plug
SDR	Shrunk Delta Ribbon	0.8 mm-pitch blade 26-blade 2-row male plug

TIP
Any combination of MDR and SDR connectors are valid.

Cable composition

Structure	Impedance	Suggested Gauge
10 High-quality twisted pairs	100 ohms differential	AWG 28 (0.08 mm²à
1 Twisted pair		
4 wires	N/A	
Overall shield	80% coverage	

WARNING
Twisted pairs must be individually shielded.

TIP
This Camera Link cable is built with *10 high-quality pairs* dedicated to carry the signals of *two Channel Links*. This cable is universal, it can be used not only as the second cable in Full and 80-bit configurations having two Channel Links but also as the first and second cable in any configuration.

TIP
This Camera Link cable supports POCL and non-POCL cameras

Wiring

Conductor	Signal*	Camera Pin#	Frame Grabber Pin#	Function*
Shield	SGND	Shell clamp	Shell clamp	EMC shield
HQ pair	Yclk+	18	9	Channel Link Y clock (Pos)
	Yclk-	5	22	Channel Link Y clock (Neg)
HQ pair	Y0+	15	12	Channel Link Y data 0 (Pos)
	Y0-	2	25	Channel Link Y data 0 (Neg)
HQ pair	Y1+	16	11	Channel Link Y data 1(Pos)
	Y1-	3	24	Channel Link Y data 1 (Neg)
HQ pair	Y2+	17	10	Channel Link Y data 2 (Pos)
	Y2-	4	23	Channel Link Y data 2 (Neg)
HQ pair	Y3+	19	8	Channel Link Y data 3 (Pos)
	Y3-	6	21	Channel Link Y data 3 (Neg)
HQ pair	Zclk+	24	3	Channel Link Z clock (Pos)
	Zclk-	11	16	Channel Link Z clock (Neg)
HQ pair	Z0+	21	6	Channel Link Z data 0(Pos)
	Z0-	8	19	Channel Link Z data 0 (Neg)
HQ pair	Z1+	22	5	Channel Link Z data 1(Pos)
	Z1-	9	18	Channel Link Z data 1 (Neg)
HQ pair	Z2+	23	4	Channel Link Z data 2 (Pos)
	Z2-	10	17	Channel Link Z data 2 (Neg)
HQ pair	Z3+	25	2	Channel Link Z data 3 (Pos)
	Z3-	12	15	Channel Link Z data 3 (Neg)
Pair	TERM	7	20	
	TERM	20	7	
Wire	Power	1	1	Power (nominal 12V DC)
Wire	GND	14	14	Power Return
Wire	GND	13	13	Power Return
Wire	Power	26	26	Power (nominal 12V DC)

NOTE
(*)The signal and function columns correspond to the second cable used in Full and 80-bit configurations.

NOTE
This wiring does not implement a straightforward pin-to-pin connection. However, the pin assignment is such that the cable can be installed in any direction.

Base/Medium Camera Link Cable

Cable Connectors

Designator	Connector family	Description
MDR	Mini Delta Ribbon	1.27 mm-pitch blade 26-blade 2-row male plug
SDR	Shrunk Delta Ribbon	0.8 mm-pitch blade 26-blade 2-row male plug

TIP
Any combination of MDR and SDR connectors are valid.

Cable composition

Structure	Impedance	Suggested Gauge
5 High-quality twisted pairs	100 ohms differential	AWG 28 (0.08 mm²à
6 Twisted pairs		
4 wires	N/A	
Overall shield	80% coverage	

WARNING
Twisted pairs must be individually shielded.

WARNING
This Camera Link cable is built with *5 high-quality pairs* dedicated to carry the signals of a *single Channel Link*. Consequently, this cable cannot be used as the second cable in Full and 80-bit configurations having two Channel Links.

TIP
This Camera Link cable supports POCL and non-POCL cameras

Wiring

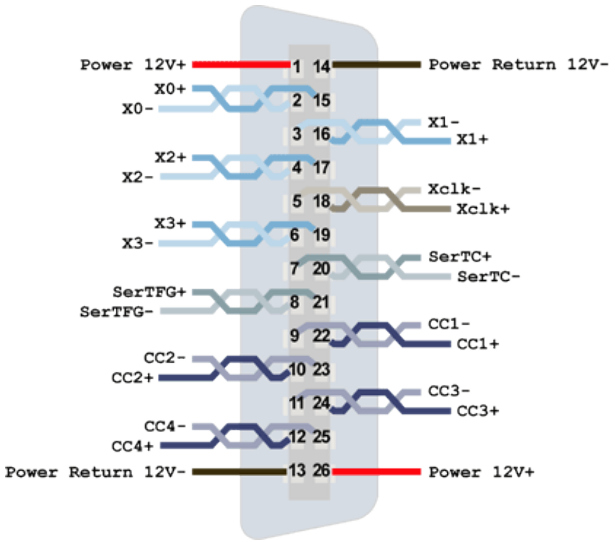
Conductor	Signal*	Camera Pin#	Frame Grabber Pin#	Function*
Shield	SGND	Shell clamp	Shell clamp	EMC shield
HQ pair	Xclk+	18	9	Channel Link clock (Pos)
	Xclk-	5	22	Channel Link clock (Neg)
HQ pair	X0+	15	12	Channel Link data 0 (Pos)
	X0-	2	25	Channel Link data 0 (Neg)
HQ pair	X1+	16	11	Channel Link data 1(Pos)
	X1-	3	24	Channel Link data 1 (Neg)
HQ pair	X2+	17	10	Channel Link data 2 (Pos)
	X2-	4	23	Channel Link data 2 (Neg)
HQ pair	X3+	19	8	Channel Link data 3 (Pos)
	X3-	6	21	Channel Link data 3 (Neg)
Pair	CC1+	22	5	Camera Control 1 (Pos)
	CC1-	9	18	Camera Control 1 (Neg)
Pair	CC2+	10	17	Camera Control 2 (Pos)
	CC2-	23	4	Camera Control 2 (Neg)
Pair	CC3+	24	3	Camera Control 3 (Pos)
	CC3-	11	16	Camera Control 3 (Neg)
Pair	CC4+	12	15	Camera Control 4 (Pos)
	CC4-	25	2	Camera Control 4 (Neg)
Pair	SerTC+	7	20	Serial to Camera (Pos)
	SerTC-	20	7	Serial to Camera (Neg)
Pair	SerTFG+	21	6	Serial to Grabber (Pos)
	SerTFG-	8	19	Serial to Grabber (Neg)
Wire	Power	1	1	Power (nominal 12V DC)
Wire	GND	14	14	Power Return
Wire	GND	13	13	Power Return
Wire	Power	26	26	Power (nominal 12V DC)

NOTE

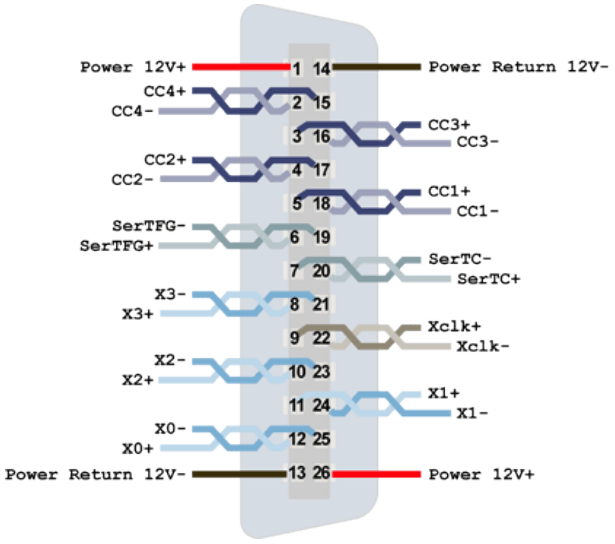
(*)The signal and function columns correspond to the cable used in a Base configuration and the first cable of a Medium configuration.

This wiring does not implement a straightforward pin-to-pin connection. However, the pin assignment is such that the cable can be installed in any direction.

Layout



Camera Link PoCL connector (cable side of the connector connected to the camera)



Camera Link PoCL connector (cable side of the connector connected to the board)