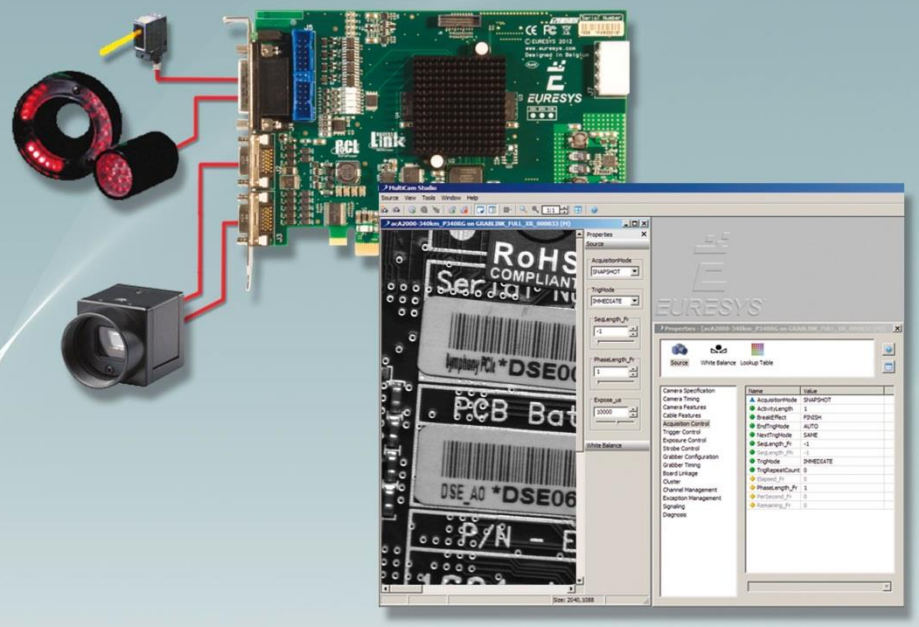
MultiCam™

Using the I/O ports of Grablink Base/DualBase/Full/Full XR

Version 1.2 December 17, 2013



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Revision History

Date	Revision	Author	Changes
2010-11-30	1.0	FL	First edition
2013-10-30	1.1	FL	Add Grablink Full XR card Add “Interconnecting Grablink Cards Using Isolated I/O’s” sections Add Grablink 3G System I/O structure Add Sync Bus and Event Outputs
2013-12-17	1.2	FL	Change template for publication on Euresys Web Site

Table of contents

1 Foreword

This document targets system designers willing to use the I/O ports of the following Grablink cards: Grablink Full, Grablink Full XR, Grablink DualBase, and Grablink Base.

In this document "Grablink card" designates any of the above mentioned cards

2 Description

2.1 I/O sets

Every acquisition channel owns 1 set of I/O ports:

- Grablink Full, Grablink Full XR, and Grablink Base own only **one (1)** set of I/O ports
- Grablink DualBase owns **two (2)** sets of I/O ports.

Each I/O set provides **ten (10)** I/O ports:

- 2 high-speed differential input ports,
- 4 isolated current-sense input ports, and
- 4 isolated output ports.

Note:

1. *There are no bidirectional I/O ports.*
2. *An acquisition channel has only access to the I/O ports that it owns! Consequently:*
    a. *There is no I/O resource allocations issue!*
    b. *An I/O port cannot be shared by multiple acquisition channels even when they belong to the same card (for instance: Grablink DualBase)!*

2.2 I/O connectors

2.2.1 Internal I/O connector

On all cards, there is one 26-pin standard-pitch flat-cable header connector for each acquisition channel that provides the connections for all the 10 I/O ports, 5V, and 12V power outputs.

Note:

1. *All the internal I/O connectors exhibit a uniform pin layout, facilitating the migration between cards!*
2. *The internal I/O connector is exclusively accessible from the inside of the PC chassis.*

2.2.2 Grablink Full and Grablink Full XR external I/O connector

On Grablink Full and Grablink Full XR, all the I/O ports, the 5V, and the12V power outputs are also available on a connector mounted on the bracket.

The connector is a robust High-Density 3-row 26-pin female Sub-D connector equipped with UNC4-40 screw locks to firmly attach the cable on the bracket.

2.2.3 Grablink DualBase external I/O connector

On Grablink DualBase, a selection of the I/O ports of both acquisition channels, the 5V, and the 12V power outputs are also available on a connector mounted on the bracket.

The connector type is the same as for Grablink Full and Grablink Full XR: A robust High-Density 3-row 26-pin female Sub-D connector equipped with UNC4-40 screw locks to firmly attach the cable on the bracket.

The pin layout is similar to the pin layout of the Grablink Full and Grablink Full XR external I/O connector: The I/O ports belonging to acquisition Channel-A and the 5V and 12V power outputs occupy the same position on the connector.

2.2.4 Grablink Base external I/O connector

The Grablink Base can be fitted with one of the following brackets:

- A Standard profile bracket that exhibits 1 camera connector and 1 external I/O connector fitted with a flat cable terminated with a 25-pin connector.
- A Low profile bracket that exhibits only 1 camera connector.

When a Grablink Base is configured with the standard profile bracket, it is possible to re-route all the I/O ports and the 5V/12V power outputs to the Sub-D25 connector mounted on the bracket. This is achieved by plugging the 26-pin connector of the flat cable into the internal I/O connector.

The external I/O connector is a robust 2-row 25-pin female Sub-D connector equipped with UNC4-40 screw locks to firmly attach the cable on the bracket.

2.3 I/O electrical characteristics

2.3.1 Overview

There are two types of electrical circuits for the input ports:

- Isolated current sense input
- High-speed differential input

There is one type of electrical circuit for the output ports:

- Isolated contact output

Note:

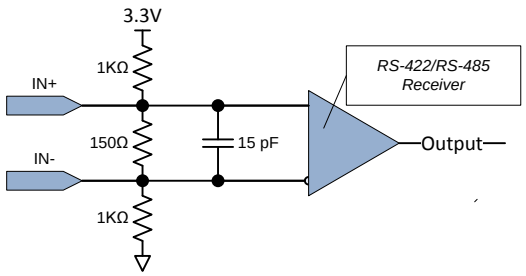
1. *Each port makes use of 2 electrical lines that allows better common mode rejection than ground referred inputs.*
2. *All the ports but the "High-speed differential input" ports are individually isolated*
3. *There are no jumpers or switches; the I/O ports don't require any hardware configuration*

2.3.2 High-speed differential inputs

Source: electrical specifications section of the handbook

High-speed differential input

Simplified schematic



The high-speed differential input ports exhibit the following characteristics:

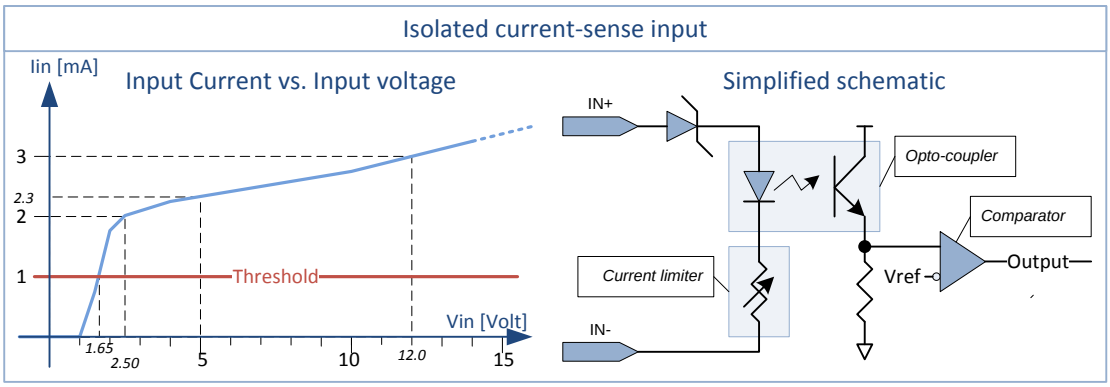
- Non-isolated ANSI/TIA/EIA-422-B differential line receiver
- -7V / +12V common mode voltage
- 4 kV contact, 8 kV air discharge ESD protection
- Minimum pulse width: 100 nanoseconds
- Maximum 10%-90% rise/fall time: 1 us
- Maximum pulse rate: 5 MHz
- Fixed termination of 120 Ohms
- Guaranteed 'HIGH' input state when unconnected (hardware failsafe circuit)
- HF Noise analog and digital filters

The state of the port is reported as follows into the `InputState.xx` MultiCam parameter:

Input voltage	InputState
$(V_{IN+} - V_{IN-}) > V_{Threshold}$	HIGH
$(V_{IN+} - V_{IN-}) < V_{Threshold}$	LOW
Unconnected input port	HIGH

2.3.3 Isolated current-sense inputs

Source: electrical specifications section of the handbook



The isolated current-sense input ports exhibit the following characteristics:

- Current-sense input:
  - Input Current Threshold: 1mA not adjustable
  - Input Voltage Threshold: 1.65 V; adjustable using an external resistor
    - Maximum low-level input voltage: 1.5V (over 0° ~70°C temperature range)
    - Minimum high-level input voltage: 1.9V (over 0° ~70°C temperature range)
  - Current limitation: max input current of 5 mA @ 30V input voltage
- Polarized input, protected against polarity reversal
- Accepts forward and reverse input voltage up to 30V without damage
- Galvanic isolation:
  - each input is individually isolated
  - isolation voltage: 500 VAC RMS
- Minimum pulse width: 10 microseconds
- Maximum pulse rate: 50 kHz
- Guaranteed 'LOW' input state when unconnected

The state of the port is reported as follows into the InputState.xx MultiCam parameter:

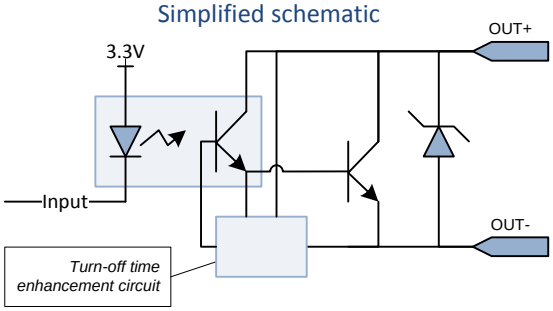
Input current	InputState
I_{IN} > 1 mA	HIGH
I_{IN} < 1 mA	LOW
Unconnected input port	LOW

2.3.4 Isolated contact output

Source: electrical specifications section of the handbook

Isolated contact output

Simplified schematic



The isolated contact output ports exhibit the following characteristics:

- Isolated contact
- Polarized output
- Galvanic isolation
  - each output is individually isolated
  - isolation voltage: 500VAC RMS
- Maximum current: 100 mA
- Maximum open state voltage (measured across pins): +/- 30V
- Maximum closed state voltage(measured across pins):
  - 1 V @ 100mA
  - 0.4 V @ 1 mA (same as for LVTTL driver)
- Fast switching speed:
  - 5 us (or better) turn-ON and turn-OFF time
  - 100 kHz max frequency
  - Typical switching performance @ 25°C

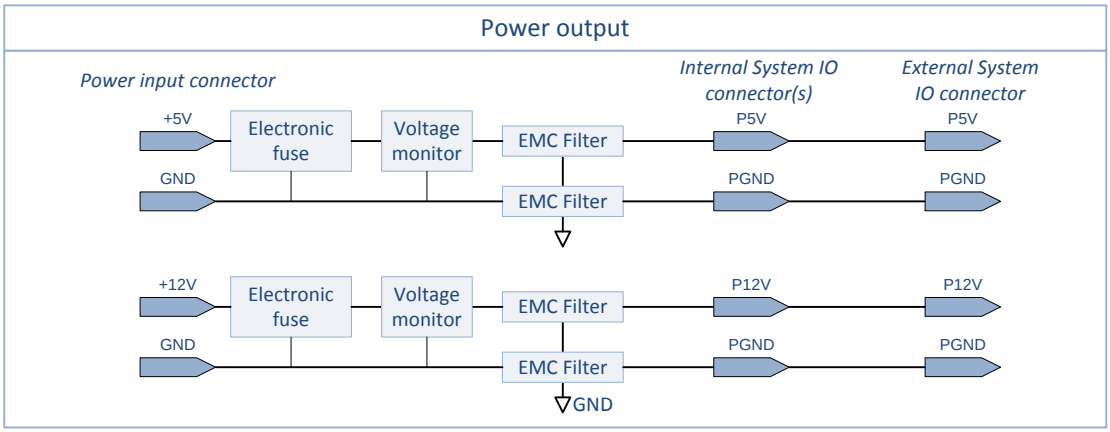
Current [mA]	Turn ON time delay [µs]	Turn OFF time delay [µs]
0.5	2.0	4.8
1.0	2.0	3.9
4.0	2.2	3.3
10	2.3	2.7
40	2.3	2.7
100	2.3	2.7

- Remains in the OFF-state until the port is under control of the application

The state of the output port is determined as follows by the `OutputState.xx` MultiCam parameter:

OutputState	Output port state
HIGH	The contact switch is closed (ON)
LOW	The contact switch is open (OFF)
Initial state after Power-On	The contact switch is open (OFF)

2.3.5 Power supply output



Non-isolated +5V and +12V power outputs are available on all the I/O connectors.

The power originates from a 4-pin Hard Disk Power Supply connector and NOT from the PCI Express connector. It is then mandatory to connect a Hard Disk power supply cable to that connector if an application requires one or both of these power outputs.

The power supply outputs are protected by electronic fuses. Such circuit, not only protects the printed circuit card against damage, but also, avoids any perturbation on the system power supply during power on sequence and also in case of overload and short-circuits on the outputs.

The sum of the load currents drawn from the 5V outputs of the I/O connectors must be lower or equal to 1.0 Amp over the whole operating temperature range of the card.

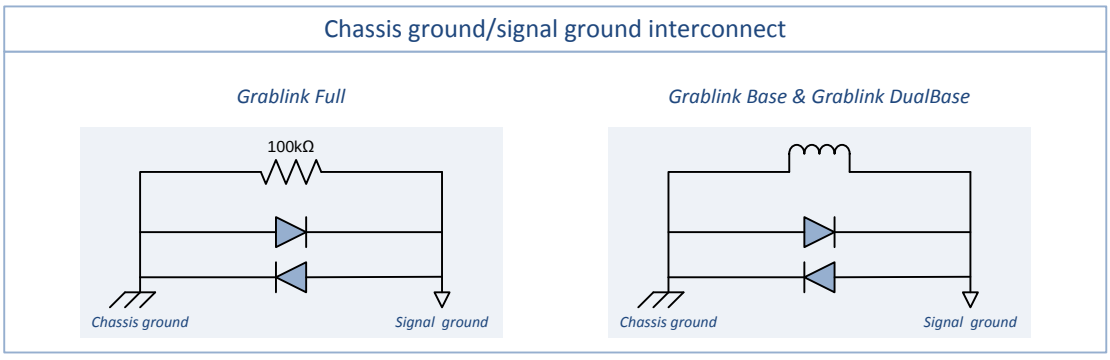
The sum of the load currents drawn from the 12V outputs of the I/O connectors must be lower or equal to 1.0 Amp over the whole operating temperature range of the card.

The presence of +5V and +12V voltages on the power output pins is reported by the voltage monitors through input ports POWER_5V and POWER_12V of the I/O system.

The input state of the POWER_5V and POWER_12V input ports is set to HIGH when the voltage across the load exceeds the "Threshold voltage". The threshold voltages are:

- 3.1 V (+/- 1.3V) for the +5V power output
- 7.3 V (+/- 3.1V) for the +12V power output

2.3.6 Chassis ground/signal ground interconnect



The "Chassis ground" electrical net is connected to the "Signal ground" electrical net through a network described here above. This prevents against significant voltages to be developed between the two nets.

On the cards having the Camera Link® PoCL feature, namely Grablink Base and Grablink DualBase, the 100 kΩ resistor is replaced by an inductor. Together with the cable shield, it provides an additional path for the (DC) return current of the camera power supply.

Note:

- *The "Chassis ground" net includes, the metallic bracket and the metallic shell of the connectors mounted on the bracket.*
- *The "Signal ground" net is actually the reference potential for all the on-card electric circuits.*

Recommendation:

- *It is mandatory to firmly attach the bracket on the chassis by means of the screw. This establishes a good electrical path between the card bracket and the chassis of the PC and hence avoids excessive current into the diodes.*

3 Electrical circuits

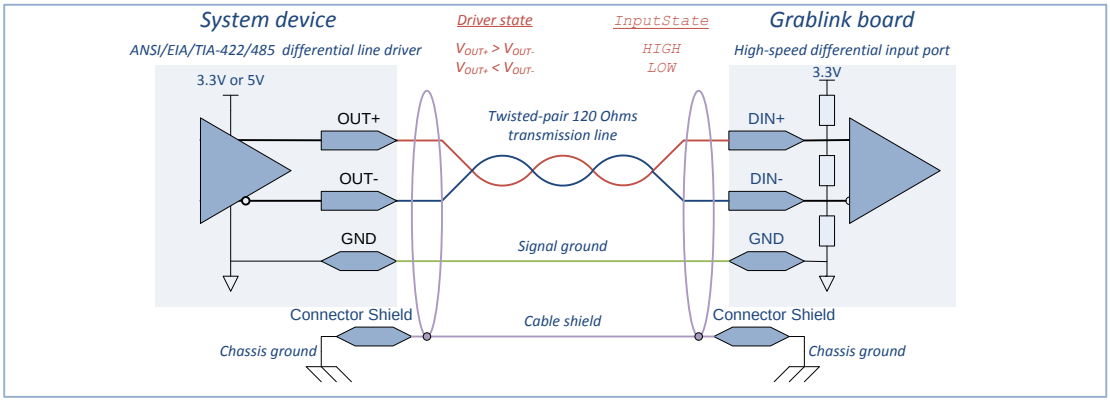
This section shows electrical circuits examples using the 3 types of I/O ports.

Notice for all cases shown hereafter

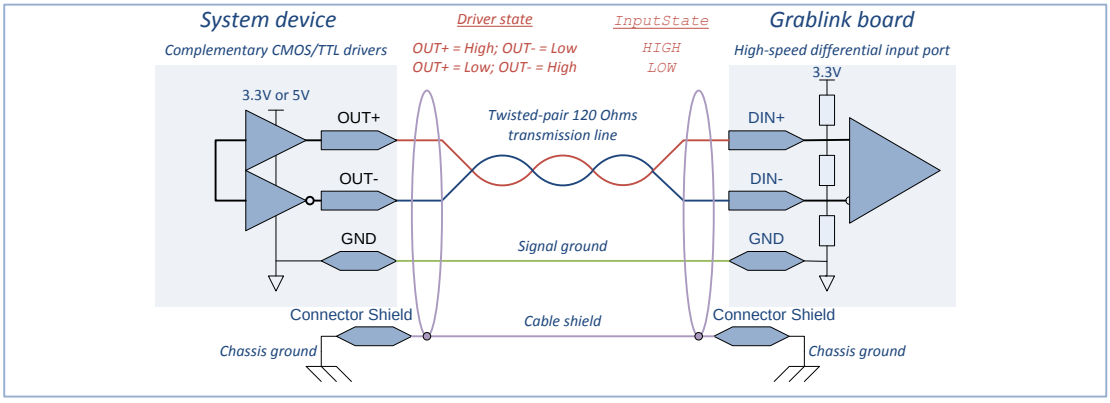
- *For better immunity to electromagnetic noise, it is recommended to use overall shielded cables and connectors that interconnect the "Chassis Ground" of each system device and the Grablink card.*

3.1 High-speed differential input ports

The following drawing shows the recommended wiring diagram for a system device using **RS-422 differential drivers**. This is the typical use case for fast system devices such as motion encoders operating at frequencies up to 5 MHz:



The following drawing shows the recommended wiring diagram for a system device using **two complementary CMOS or TTL drivers**. This is an alternate use case for fast system devices such as motion encoders operating at frequencies up to 5 MHz:



Notice that for the two above cases:

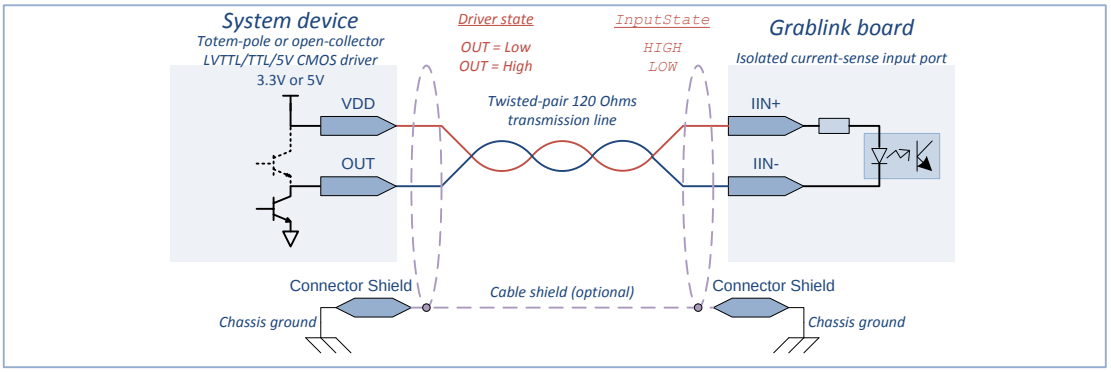
- *For correct operation of the circuit, it is mandatory to satisfy the common-mode voltage requirements of the receiver. Practically, this requirement can be achieved by the addition of one "Signal Ground" wire between each system device and the Grablink card.*

3.2 Isolated current-sense input ports

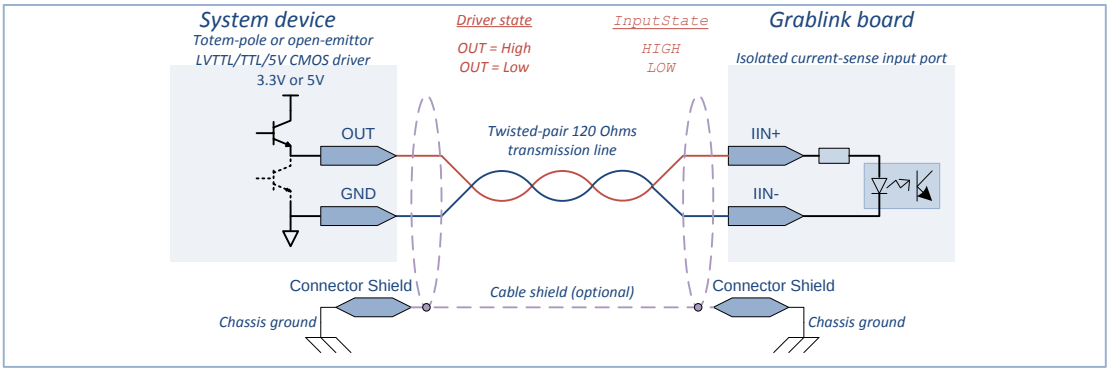
3.2.1 3V3 or 5V logic drivers

This section shows electrical circuit's examples for system devices using low-voltage 3V3 or 5V logic drivers and the isolated current-sense input ports of Grablink cards.

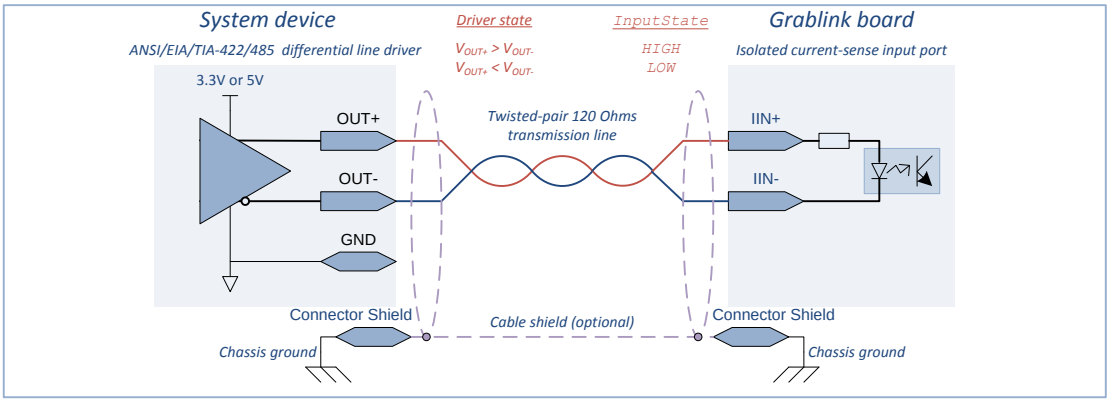
The following drawing shows the wiring diagram for a system device using **Totem-pole (or open-collector) 3.3V Low-voltage TTL, 5V TTL, or 5V CMOS drivers**. With this circuit diagram, the highest transistor of the totem-pole driver is useless:



The following drawing shows the wiring diagram for a system device using **Totem-pole (or open-emittor) 3.3V Low-voltage TTL, 5V TTL, or 5V CMOS drivers**. With this circuit diagram, the lowest transistor of the totem-pole driver is useless:



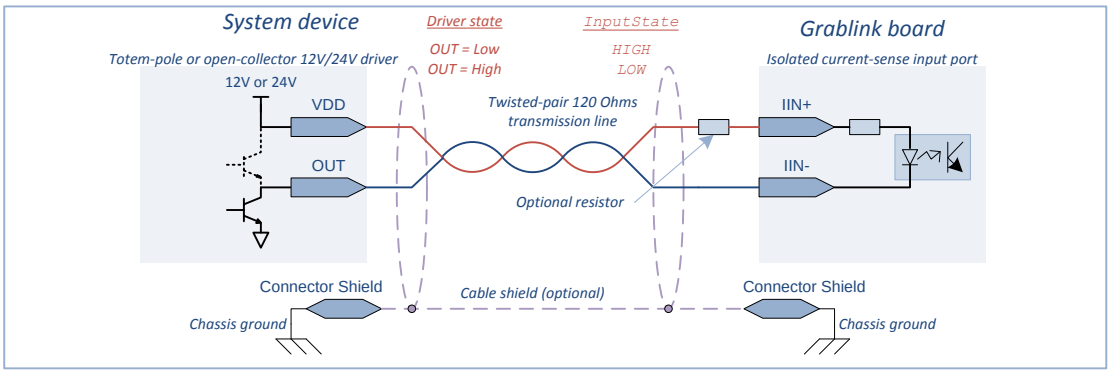
The following drawing shows an alternate wiring diagram for a system device using **RS-422 differential drivers**. This alternate solution has to be used when no more high-speed differential input ports are available and when the pulse width of the transmitted signals exceeds or equal 5 microseconds:



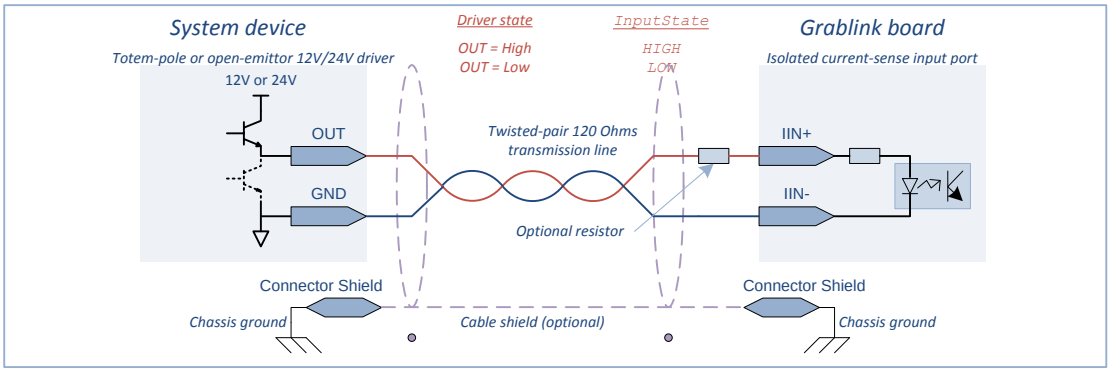
3.2.2 12V or 24V logic drivers

This section shows electrical circuit's examples for system devices using high-voltage 12V or 24V logic drivers and the isolated current-sense input ports of Grablink cards.

The following drawing shows the wiring diagram for a system device using **Totem-pole (or open-collector) 12V, or 24V CMOS drivers**. With this circuit diagram, the highest transistor of the totem-pole driver is useless:



The following drawing shows the wiring diagram for a system device using **Totem-pole (or open-emittor) 12V, or 24V CMOS drivers**. With this circuit diagram, the lowest transistor of the totem-pole driver is useless:



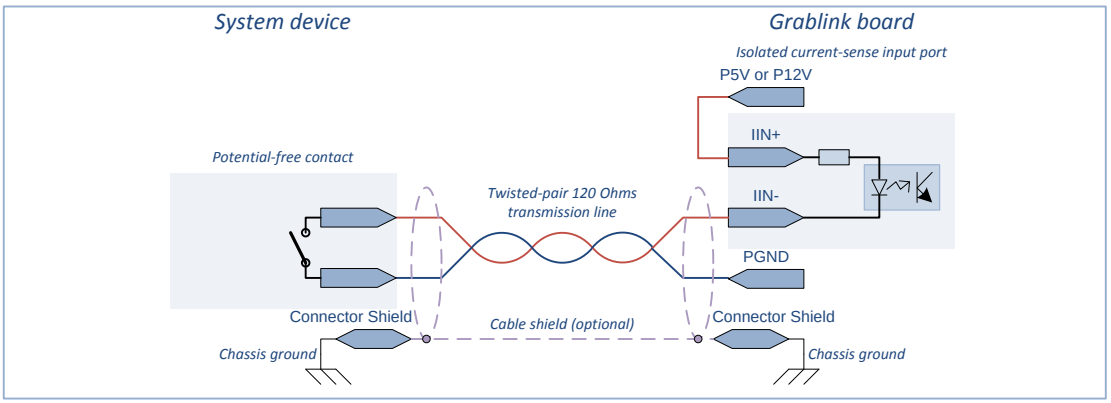
Notice for the two above cases:

- *Operation without series resistor is allowed thanks to the current limiting function of the input ports.*
- *Better noise immunity is obtained by inserting a series resistor in the circuit. The recommended resistor values are: 4.7kΩ for 12V signaling and 10kΩ for 24V signaling.*

3.2.3 Potential-free contacts

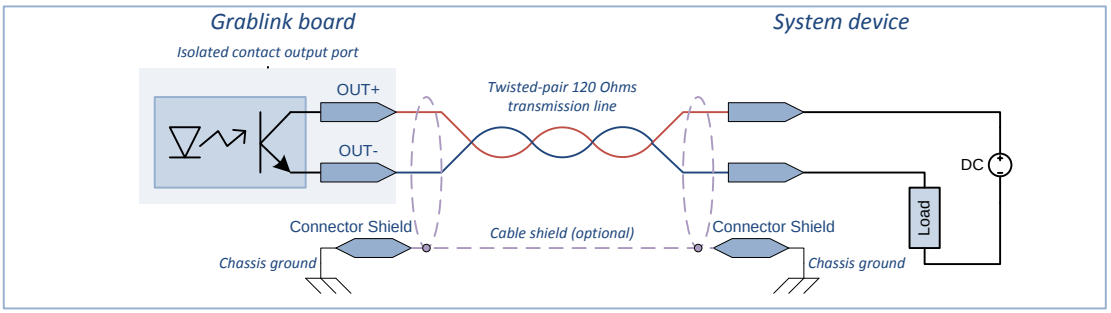
This section shows an electrical circuit example for system devices using potential-free contacts and the isolated current-sense input ports of Grablink cards.

The following drawing shows the wiring diagram for a system device using **potential-free contacts**. In this circuit, the current is supplied by the Grablink card:



3.3 Isolated contact output ports

This section shows an electrical circuit example for system devices using the isolated output port of Grablink cards. In this circuit, the current is supplied by the system device:



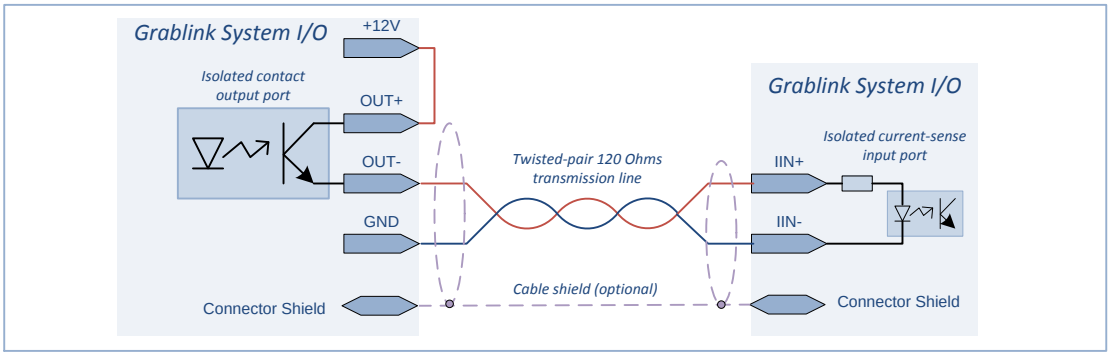
Notice that:

- *The isolated output is polarized!*
- *In case of polarity reversal, the output port acts as a closed contact.*
- *The isolated output is capable to deliver up to 100 mA and to switch voltages up to 30 V.*
- *Exceeding 100 mA or 30V may damage the output port.*
- *The +5V/+12V power may be delivered by the Grablink card.*

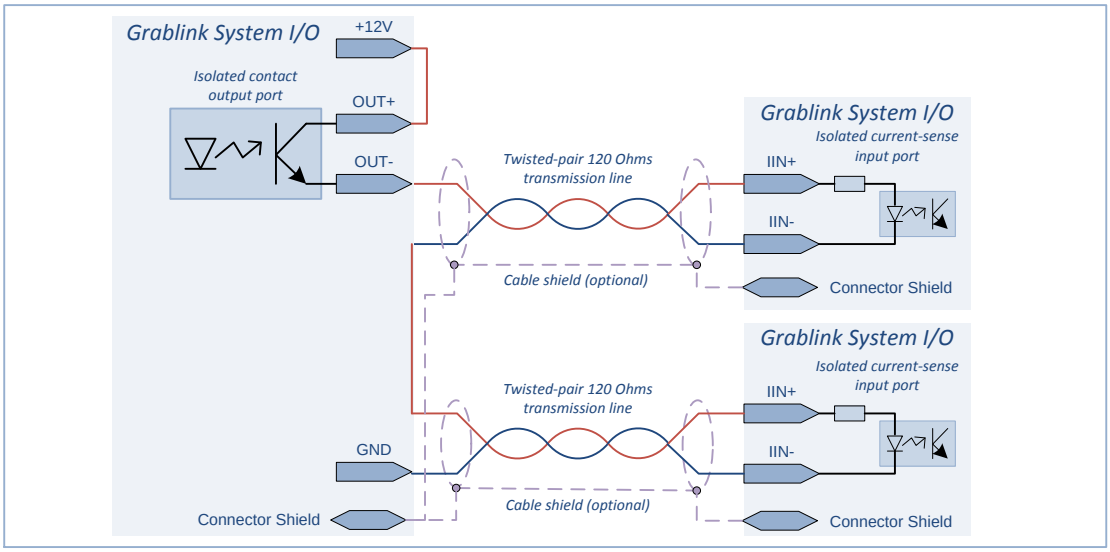
3.4 Interconnecting Grablink Cards using isolated I/O's

The following wring diagrams show two examples of Grablink cards interconnections using isolated input and output ports.

The first diagram shows a point-to-point connection:



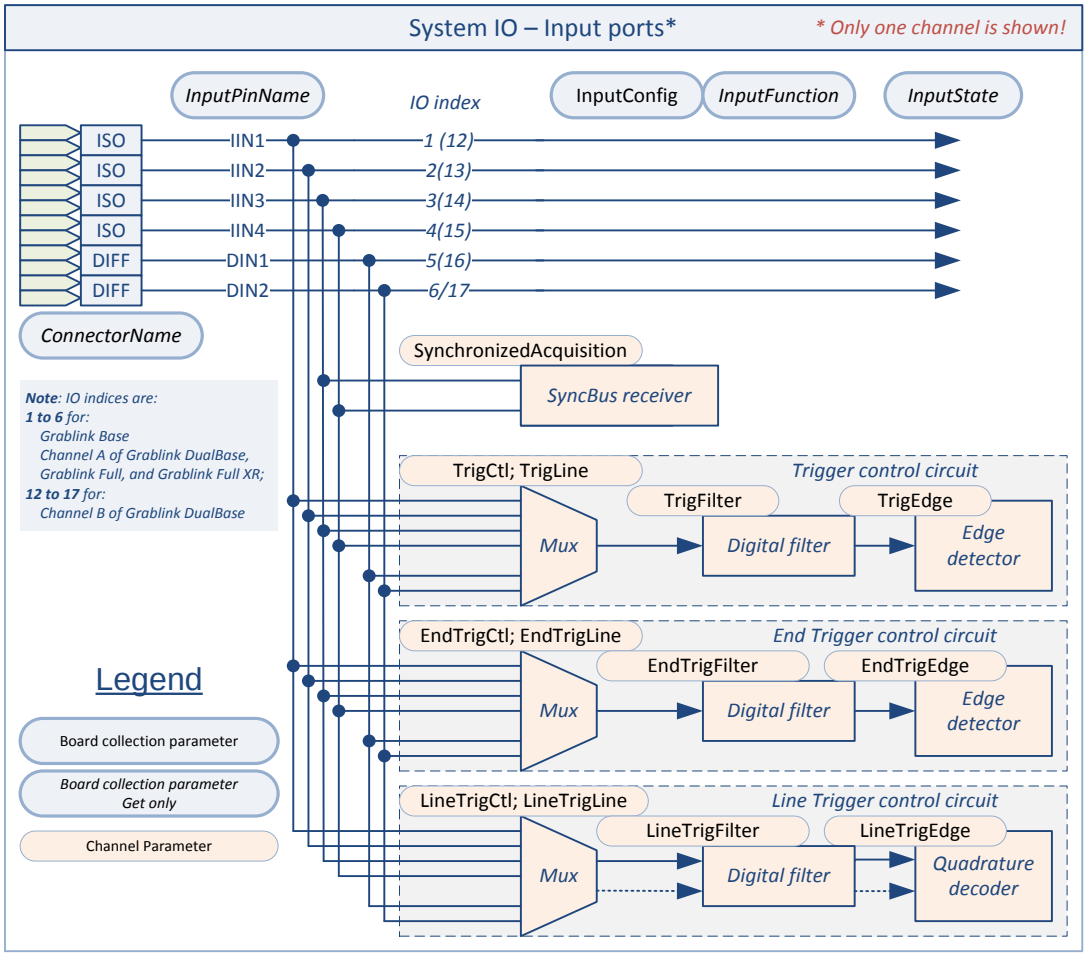
The second diagram shows a star connection of one output to two inputs:



4 Grablink System I/O Structure

4.1 Input Ports

The following drawing shows an organic diagram of the input ports of a set of System I/O:

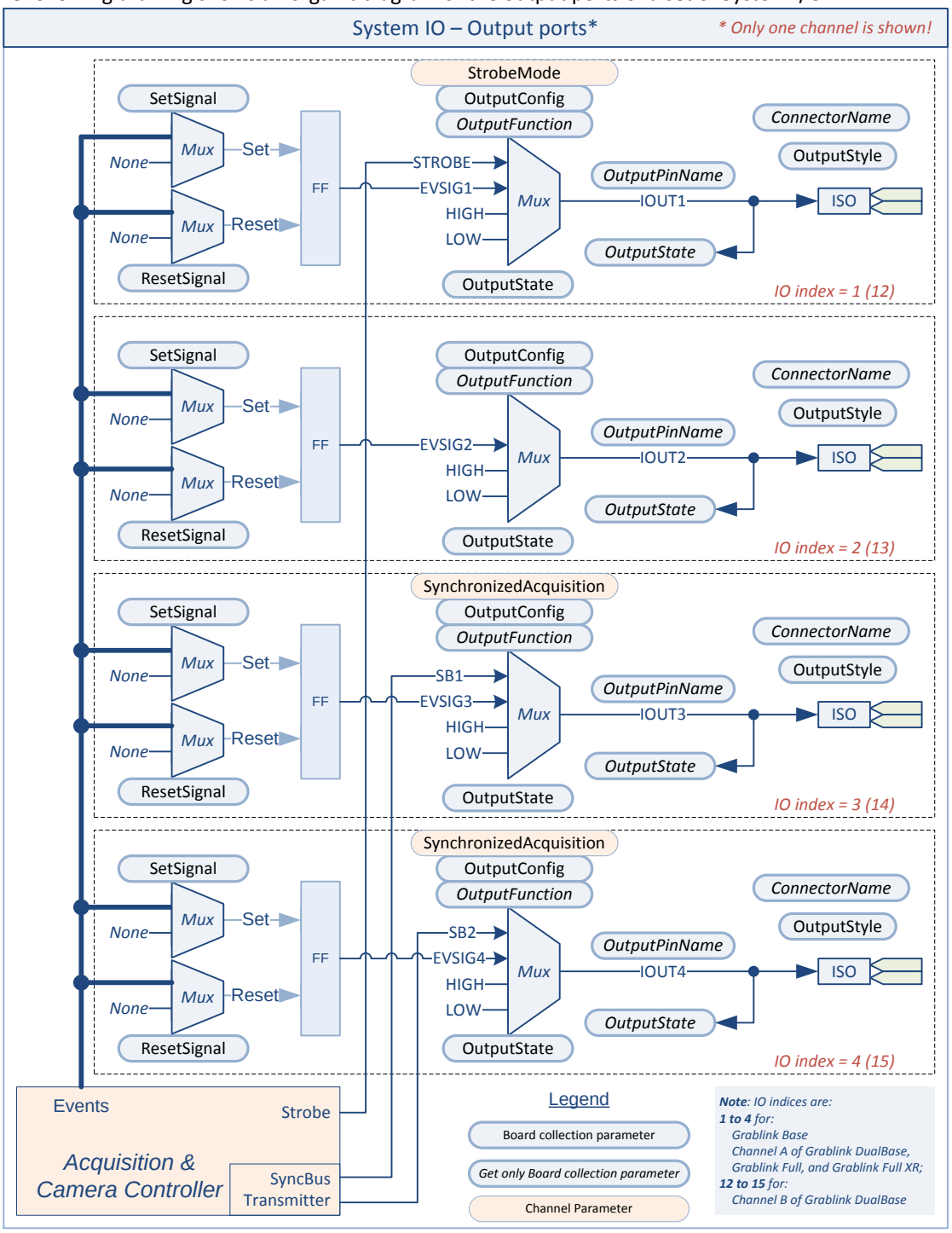


Possible usages of the input ports are:

- General purpose inputs
- SyncBus receiver
- Trigger source
- End Trigger source
- Line Trigger input

4.2 Output Ports

The following drawing shows an organic diagram of the output ports of a set of System I/O:



5 I/O Usage

5.1 Channel related functions

I/O's can be used by the MultiCam Acquisition Channel for trigger inputs, strobe output, and multi-channel synchronization purpose. For these purposes, the I/O ports are configured using the following MultiCam Channel parameters:

Channel I/O function	Function Enable/disable parameter	Electrical style parameter	Port assignment parameter
Line Trigger	LineRateMode	LineTrigCtl	LineTrigLine
Trigger	Trigmode, NextTrigMode	TrigCtl	TrigLine
End Trigger	EndTrigMode	EndTrigCtl	EndTrigLine
Strobe	StrobeMode	StrobeCtl	N/A
SyncBus Outputs	SynchronizedAcquisition	N/A	N/A
SyncBus Inputs	SynchronizedAcquisition	N/A	N/A

The following table indicates for each I/O port of an I/O set, the Channel I/O function capabilities:

I/O Port	Line Trigger Input	Line Trigger A/B Inputs	Trigger Input	End Trigger Input	SyncBus Inputs	Strobe Output	SyncBus Outputs
High-speed differential input 1	Default	Default	Alternate	Alternate	-	N/A	
High-speed differential input 2	Alternate		Default	Default	-		
Isolated input 1	Default	Default	OK	Alternate	-		
Isolated input 2	Alternate		Default	Default	-		
Isolated input 3	Alternate	Alternate	Alternate	Alternate	Fixed		
Isolated input 4	Alternate		Alternate	Alternate			
Isolated output 1	N/A					Fixed	-
Isolated output 2						-	-
Isolated output 3						-	Fixed
Isolated output 4						-	

Notice that:

- *Any of the 6 input ports (both the differential and isolated types) can be configured as Line Trigger, Trigger, or End Trigger source.*
- *Using two-phase (quadrature) motion encoders for the Line Trigger function requires the usage of two input ports. As shown in the above table, only 3 port combinations are allowed!*
- *Only the output port 1 is capable to be configured as strobe output; the other output ports can only be used as general purpose outputs*

5.2 General Purpose I/O

Every I/O port can be used as a general-purpose card I/O; in that case, it has to be configured and managed using the **MultiCam Board I/O** parameters.

5.3 Events Outputs

Every output port can be used to deliver an electrical signal built from a selection of internal events.

For that usage, the I/O ports are configured through the MultiCam Board parameters `SetSignal` and `ResetSignal`.

6 Appendix

6.1 About galvanic isolation

(Source: Wikipedia)

Galvanic isolation is the principle of isolating functional sections of electric systems so that charge-carrying particles cannot move from one section to another, i.e. there is no electric current flowing directly from one section to the next. Energy and/or information can still be exchanged between the sections by other means, however, such as by capacitance, induction, electromagnetic waves, optical, acoustic, or mechanical means.

Galvanic isolation is used in situations where two or more electric circuits must communicate, but their grounds may be at different potentials. It is an effective method of breaking ground loops by preventing unwanted current from travelling between two units sharing a ground conductor. Galvanic isolation is also used for safety considerations, preventing accidental current from reaching the ground (the building floor) through a person's body.

6.2 Electronic fuse operation

Soft Start

When establishing the power, the electronic fuse performs a soft start: the voltage across the load rises smoothly up to the nominal level. The time required to raise the voltage up to the nominal value is typically 1 millisecond for the 12V outputs and 1.4 milliseconds for the 5V outputs.

Current limiting

When the internal FET of the electronic fuse is not fully conductive, for instance during the soft-start: If the load current exceeds the "short-circuit current limit", the electronic fuse limits the output current.
When the internal FET of the electronic fuse is fully conductive, the load current may increase beyond the "short-circuit current limit" up to the "overload current limit".
If the load current reaches the "overload current limit", the electronic fuse starts reducing the load current until it reaches the "short-circuit current limit" level.
On the 5V and 12V types of electronic fuses, the "short-circuit current limit" is typically 2.0 Amp and the "overload current limit" is typically 3.2 Amp.

Overheat protection

If the electronic fuse internal temperature becomes excessive, the electronic fuse turns off completely.

Overvoltage protection

If the input voltage exceeds the "voltage limit", the electronic fuse clamps the voltage applied to the load. The typical clamp voltage is respectively 15V for the +12V output and 6.65V and for the +5V output.

Undervoltage lockout

If the input voltage drops below the "min. input voltage limit", the electronic fuse turns off completely. The typical "min. input voltage limit" is respectively 8.5V for the +12V output and 3.6V for the +5V output.