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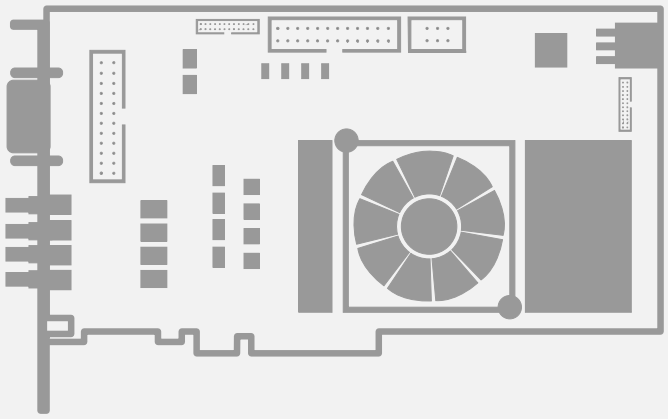
HARDWARE MANUAL

Coaxlink

Coaxlink PCIe Hardware Manual

1630 Coaxlink Mono
1631 Coaxlink Duo
1632 Coaxlink Quad
1633 Coaxlink Quad G3
1633-LH Coaxlink Quad G3 LH
1635 Coaxlink Quad G3 DF
1637 Coaxlink Quad 3D-LLE
3602 Coaxlink Octo
3603 Coaxlink Quad CXP-12
3620 Coaxlink Quad CXP-12 JPEG
3621-LH Coaxlink Mono CXP-12 LH
3622 Coaxlink Duo CXP-12



Terms of Use

This documentation is provided with Coaxlink 12.5.4 (doc build 2109).
www.euresys.com

Contents

1. About This Document

1.1. Document Scope

NOTE
This document describes the *hardware specifications* of the following products of the Coaxlink series together with their related products.

Coaxlink main products

Product	S/N Prefix	Icon
1630 Coaxlink Mono	KMO	Mono
1631 Coaxlink Duo	KDU	Duo
1632 Coaxlink Quad	KQU	Quad
1633 Coaxlink Quad G3	KQG	QuadG3
1633-LH Coaxlink Quad G3 LH	KQH	QuadG3LH
1635 Coaxlink Quad G3 DF	KDF	QuadG3DF
1637 Coaxlink Quad 3D-LLE	KQE	Quad3DLLE
3602 Coaxlink Octo	KOC	Octo
3603 Coaxlink Quad CXP-12	KQP	QuadCXP12
3620 Coaxlink Quad CXP-12 JPEG	KQJ	QuadCXP12J
3621-LH Coaxlink Mono CXP-12 LH	KMP	MonoCXP12LH
3622 Coaxlink Duo CXP-12	KDP	DuoCXP12

Related accessory products

Product	S/N Prefix	Icon
1625 DB25F I/O Adapter Cable	DBC	1625
1636 InterPC C2C-Link Adapter	KCC	1636
3303 C2C-Link Ribbon Cable		3303
3304 HD26F I/O Adapter Cable		3304
3610 HD26F I/O Extension Module TTL-RS422	EMA	3610
3612 HD26F I/O Extension Module TTL-CMOS5V-RS422	EMC	3612
3614 HD26F I/O Extension Module - Standard I/O Set	EMD	3614

NOTE
The S/N prefix is a 3-letter string at the beginning of the card serial number.

NOTE
Icons are used in this document for tagging titles of card-specific content.

1.2. Document Changes

Coaxlink 12.5

Interactive pin assignments table for all connectors (HTML only)

The following topic were revised:

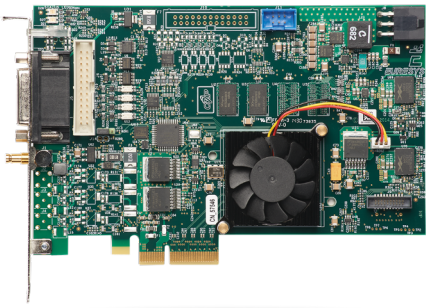
- "PCI Express Power" on page 77
- "Thermal Data" on page 104

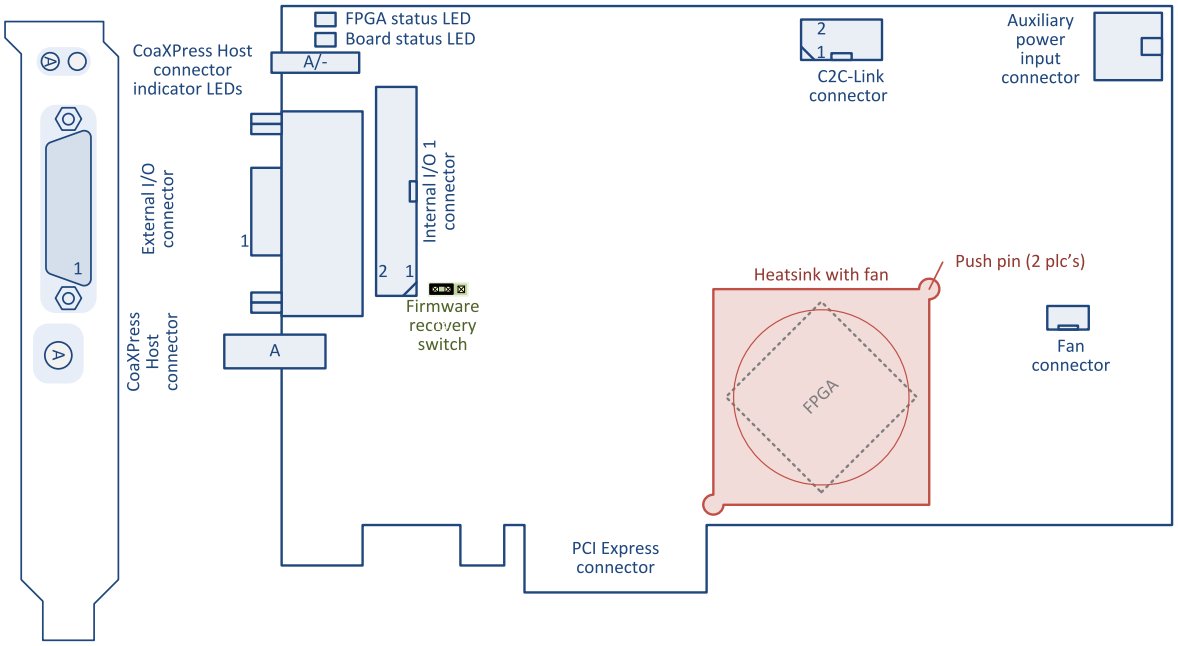
2. Mechanical Specification

Mechanical specifications of the product(s) including: product pictures, physical dimensions, connectors description and pin assignments, LEDs description, switches description, etc.

2.1. Board and Bracket Layouts

1630 Coaxlink Mono





- "DIN 1 CoaXPress Host Connector" on page 23
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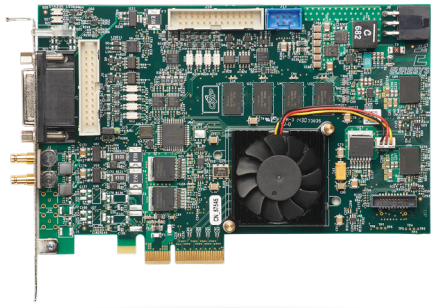
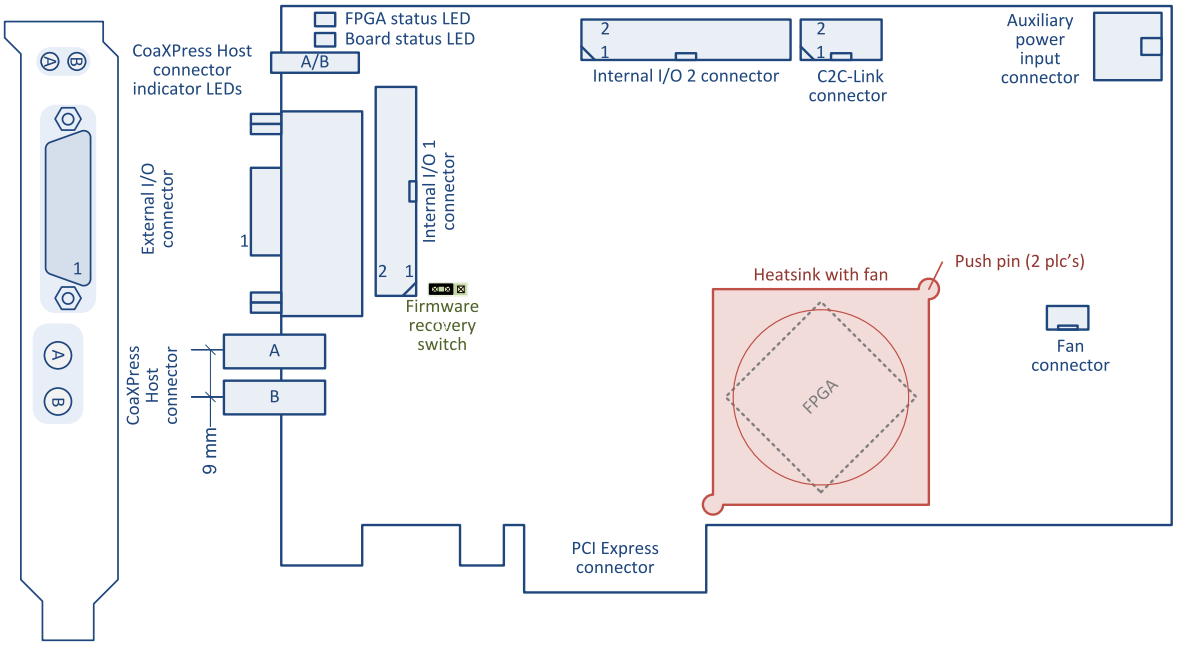
1631 Coaxlink Duo





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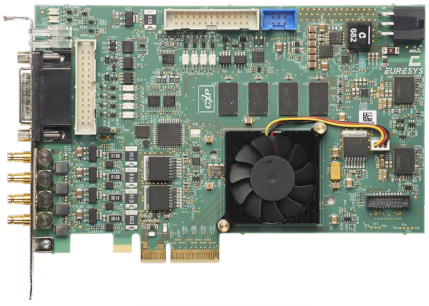
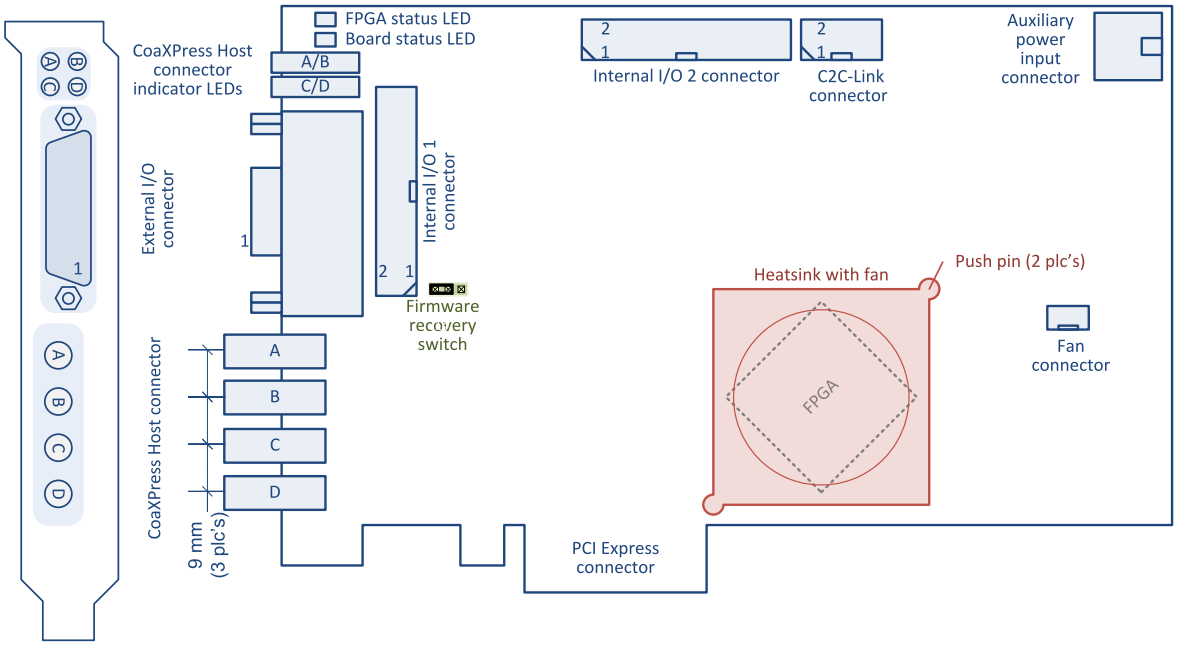
1632 Coaxlink Quad





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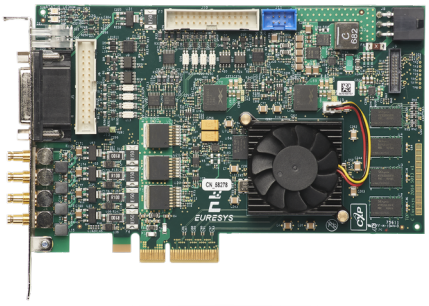
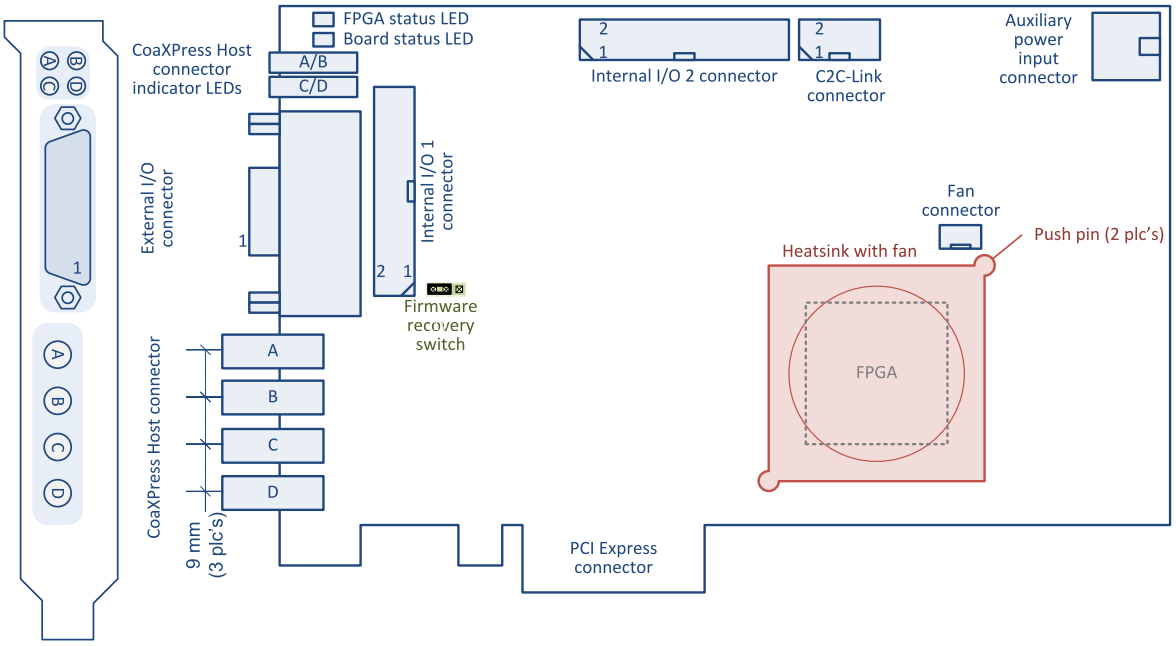
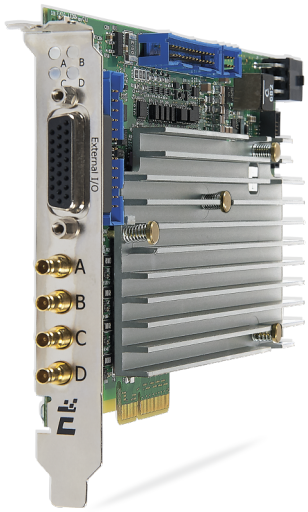
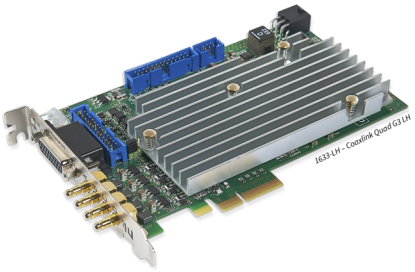
1633 Coaxlink Quad G3

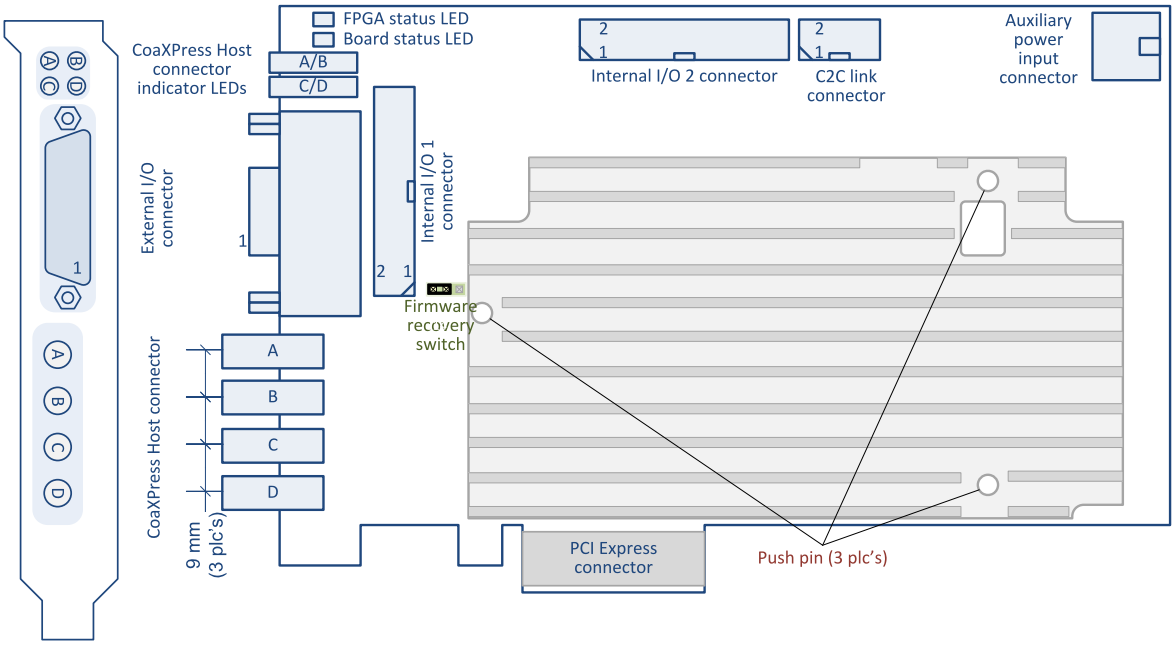




1633-LH Coaxlink Quad G3 LH







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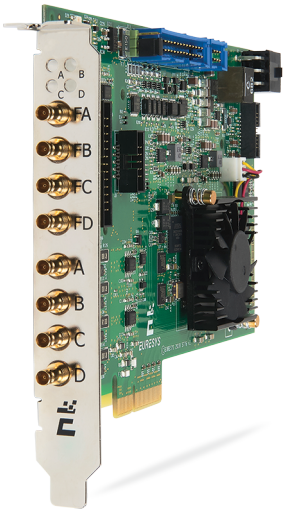
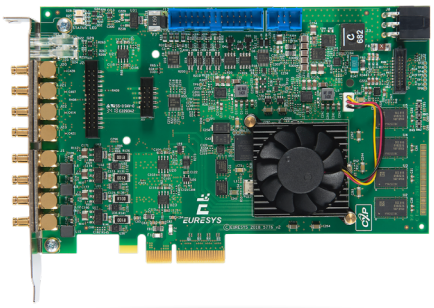
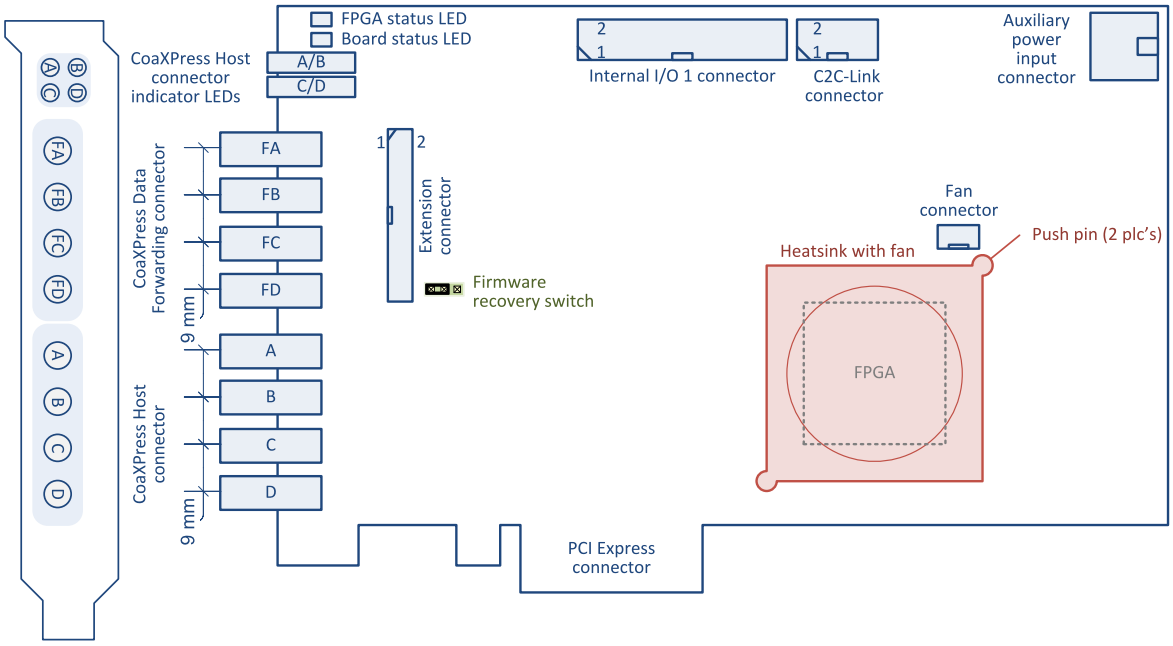
1635 Coaxlink Quad G3 DF







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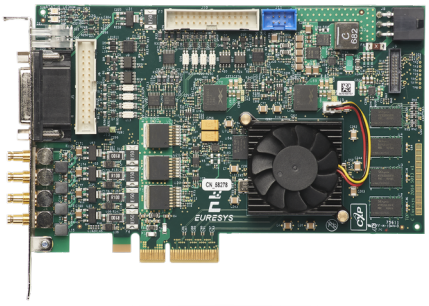
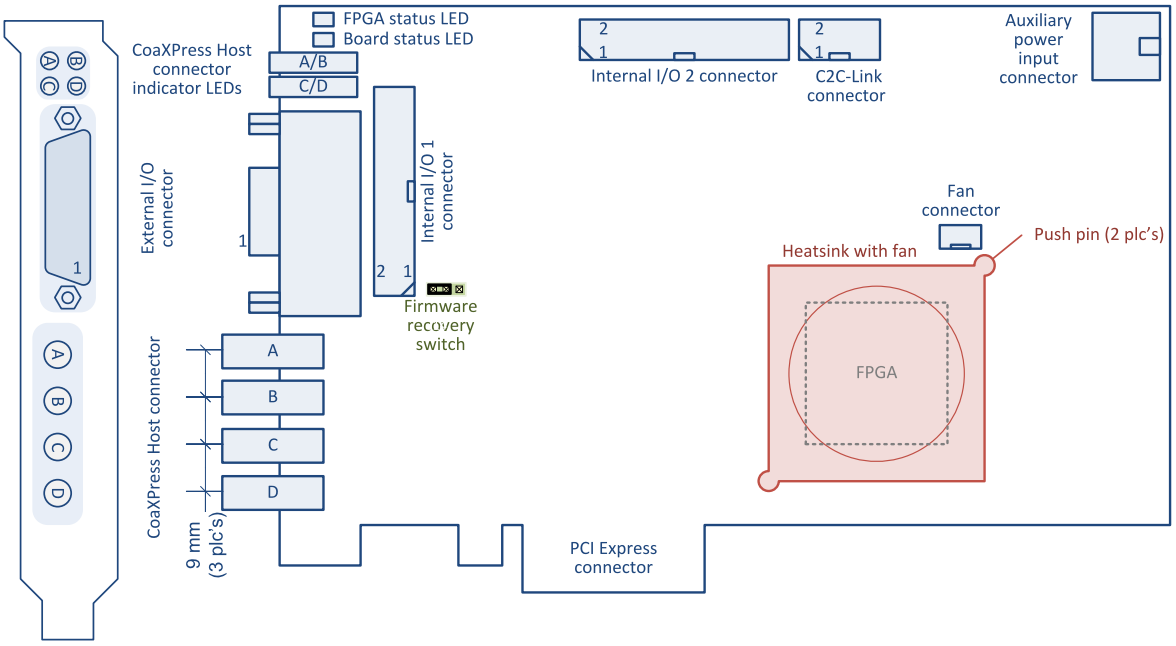
1637 Coaxlink Quad 3D-LLE





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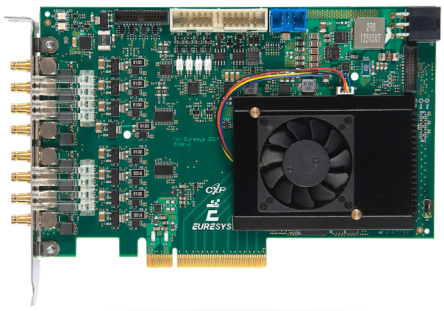
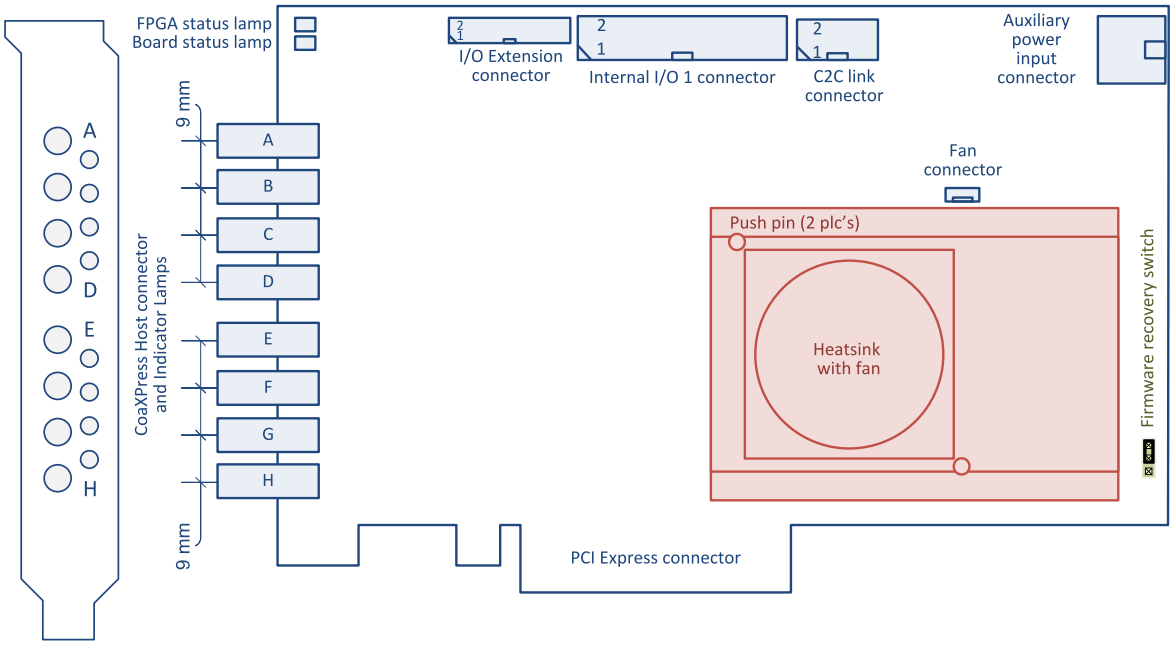
3602 Coaxlink Octo





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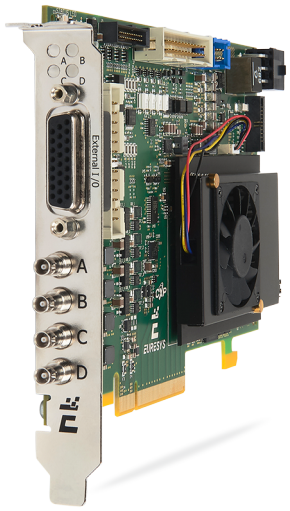
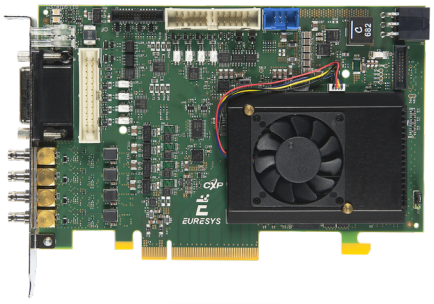
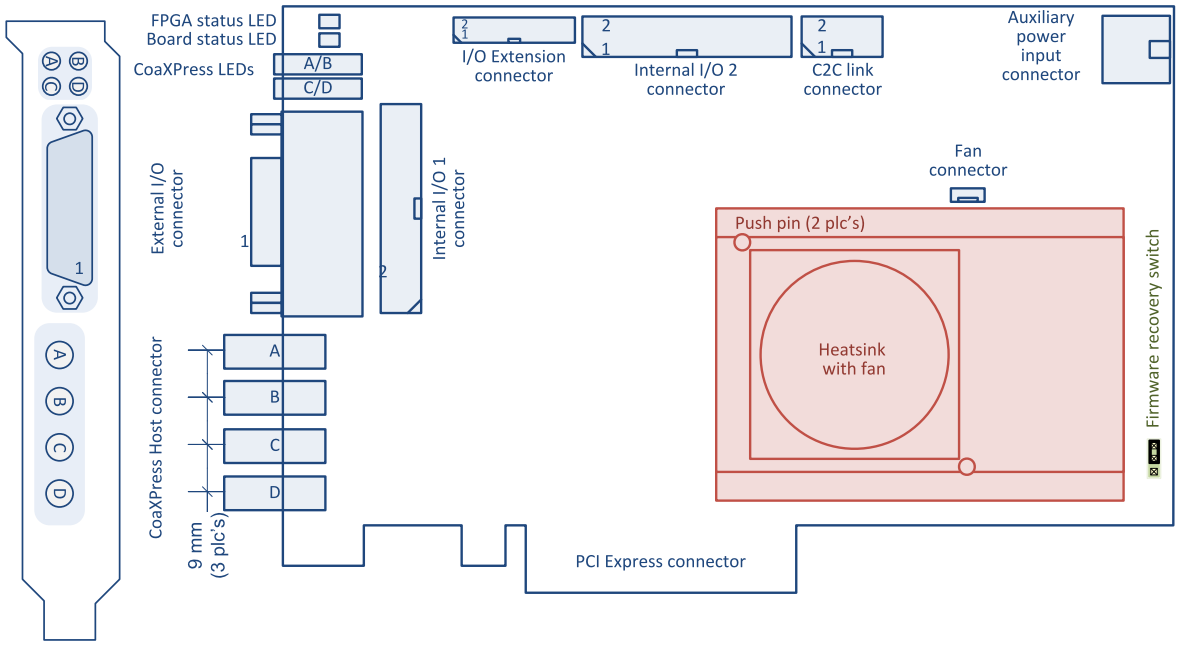
3603 Coaxlink Quad CXP-12







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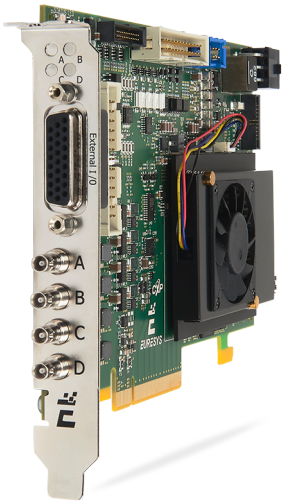
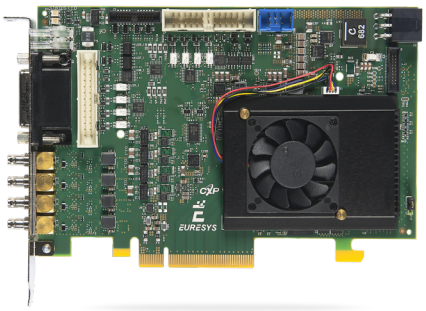
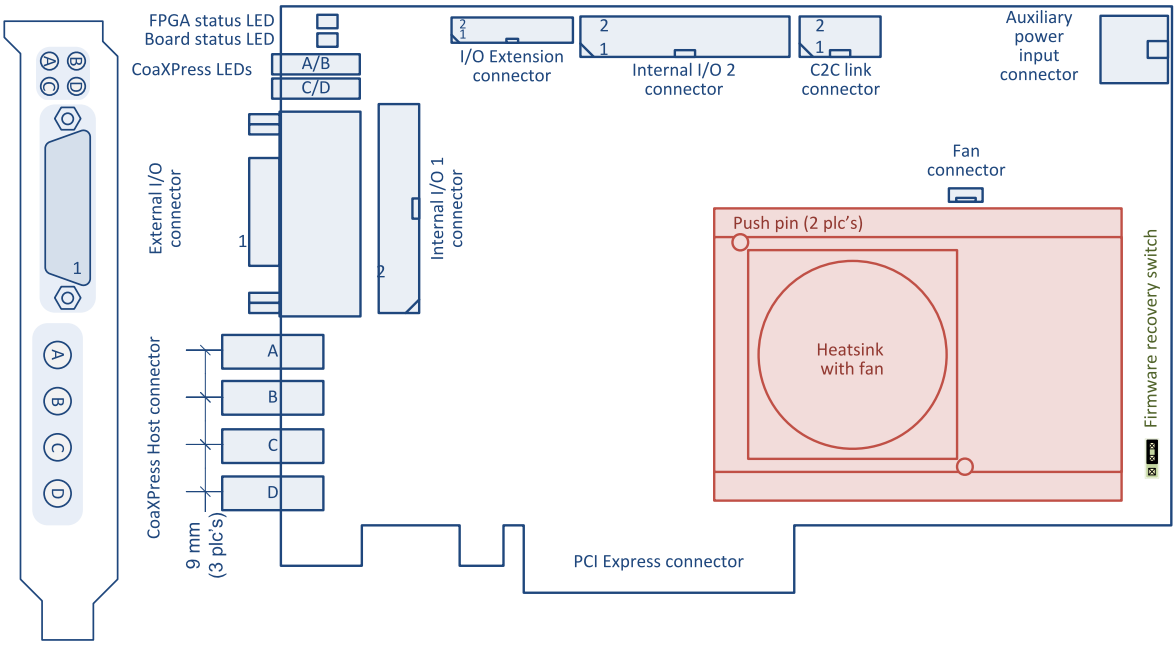
3620 Coaxlink Quad CXP-12 JPEG







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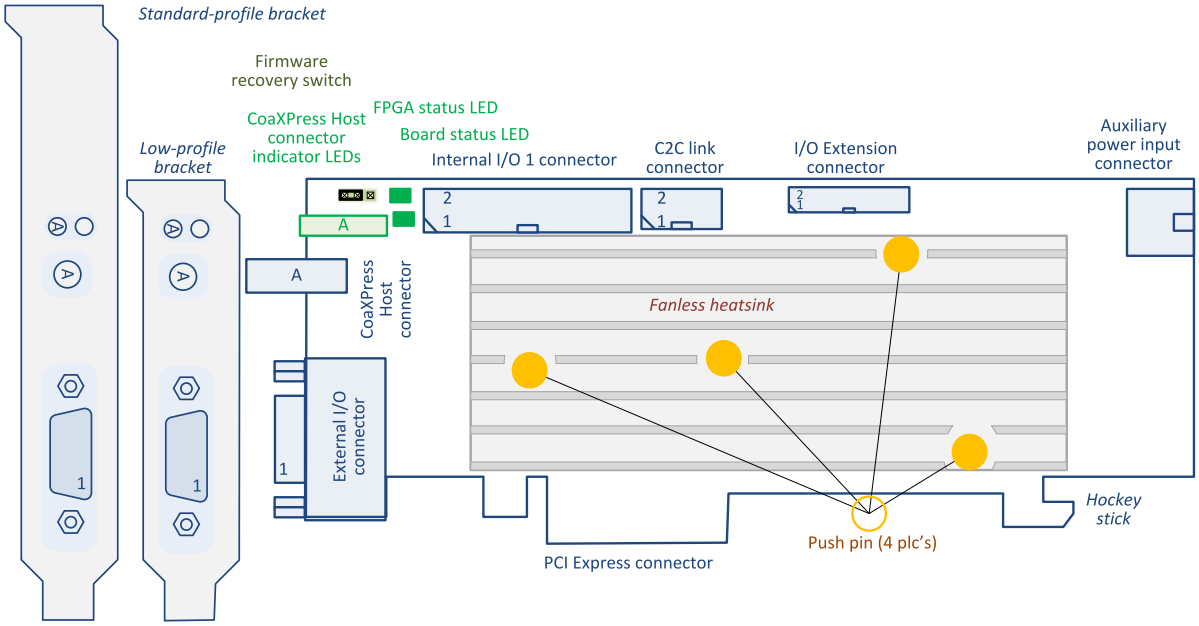
3621-LH Coaxlink Mono CXP-12 LH



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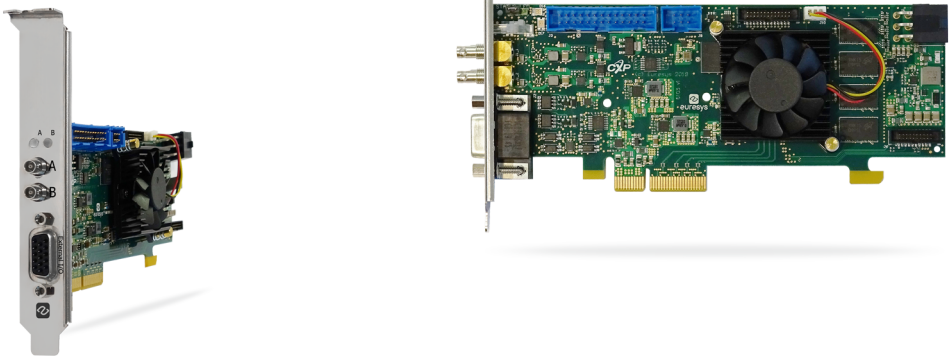
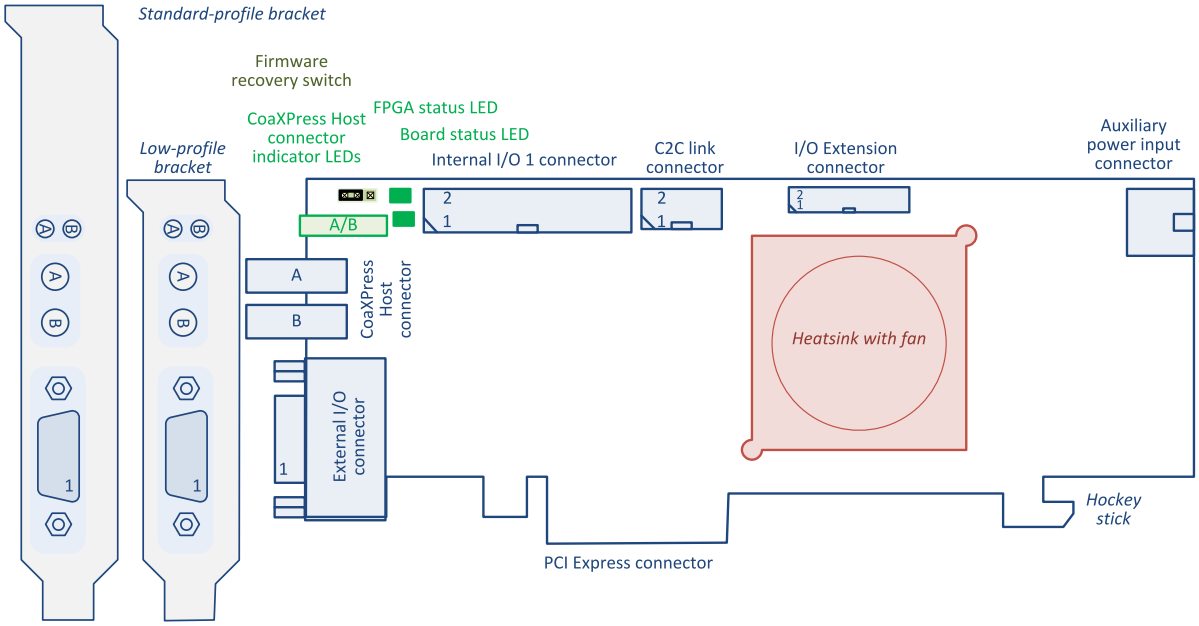
3622 Coaxlink Duo CXP-12





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2.2. Connectors

DIN 1 CoaXPress Host Connector

Applies to:
Mono

Connector description

Property	Value
Name	CoaXPress Host
Type	DIN 1.0/2.3 75 Ohms coaxial female receptacle
Location	Card bracket
Usage	CoaXPress Host Interface

Pin assignments

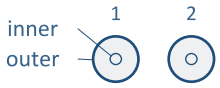
Pin	Signal	Usage
Inner	CXP_A	CoaXPress Host Connection A
Outer	GND	Ground

DIN 2 CoaXPress Host Connector

Applies to:
Duo

Connector description

Property	Value
Name	CoaXPress Host
Type	2 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Host Interface



Pin assignments

Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground

DIN 4 CoaXPress Host Connector

Applies to:

Quad | QuadG3 | QuadG3LH | QuadG3DF | Quad3DLLE

Connector description

Property	Value
Name	CoaXPress Host
Type	4 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Host Interface

Pin assignments

Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground
Inner3	CXP_C	CoaXPress Host Connection C
Outer3	GND	Ground
Inner4	CXP_D	CoaXPress Host Connection D
Outer4	GND	Ground

DIN 8 CoaXPress Host Connector

Applies to:
Octo

Connector description

Property	Value
Name	CoaXPress Host
Type	8 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Host Interface

Pin assignments

Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground
Inner3	CXP_C	CoaXPress Host Connection C
Outer3	GND	Ground
Inner4	CXP_D	CoaXPress Host Connection D
Outer4	GND	Ground
Inner5	CXP_E	CoaXPress Host Connection E
Outer5	GND	Ground
Inner6	CXP_F	CoaXPress Host Connection F
Outer6	GND	Ground
Inner7	CXP_G	CoaXPress Host Connection G
Outer7	GND	Ground
Inner8	CXP_H	CoaXPress Host Connection H
Outer8	GND	Ground

Micro-BNC 1 CoaXPress Host Connector

Applies to:
MonoCXP12LH

Connector description

Property	Value
Name	CoaXPress Host
Type	Micro-BNC 75 Ohms coaxial receptacle
Location	Card bracket
Usage	CoaXPress Host Interface

Pin assignments

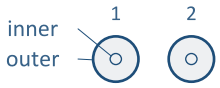
Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground

Micro-BNC 2 CoaXPress Host Connector

Applies to:
DuoCXP12

Connector description

Property	Value
Name	CoaXPress Host
Type	2 x Micro-BNC 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Host Interface



Pin assignments

Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground

Micro-BNC 4 CoaXPress Host Connector

Applies to:
QuadCXP12 QuadCXP12J

Connector description

Property	Value
Name	CoaXPress Host
Type	4 x Micro-BNC 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Host Interface

Pin assignments

Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground
Inner3	CXP_C	CoaXPress Host Connection C
Outer3	GND	Ground
Inner4	CXP_D	CoaXPress Host Connection D
Outer4	GND	Ground

CoaXPress Data Forwarding Connector

Applies to:
QuadG3DF

Connector description

Property	Value
Name	CoaXPress Data Forwarding
Type	4 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Card bracket
Usage	CoaXPress Data Forwarding Interface

Pin assignments

Pin	Signal	Usage
Inner1	CXP_FA	CoaXPress Data Forwarding Connection A
Outer1	GND	Ground
Inner2	CXP_FB	CoaXPress Data Forwarding Connection B
Outer2	GND	Ground
Inner3	CXP_FC	CoaXPress Data Forwarding Connection C
Outer3	GND	Ground
Inner4	CXP_FD	CoaXPress Data Forwarding Connection D
Outer4	GND	Ground

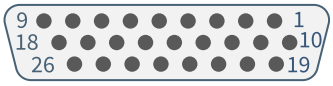
External I/O Connector

Applies to:

Mono | Duo | Quad | QuadG3 | QuadG3LH | Quad3DLLE | QuadCXP12 | QuadCXP12J

Connector description

Property	Value
Name	External I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN12+	High-speed differential input #12 – Positive pole
3	IIN11+	Isolated input #11 – Positive pole
4	IIN13-	Isolated input #13 – Negative pole
5	IIN14-	Isolated input #14 – Negative pole
6	IOUT12-	Isolated contact output #12 – Negative pole
7	GND	Ground
8		Not connected
9	GND	Ground
10	GND	Ground
11	DIN12-	High-speed differential input #12 – Negative pole
12	IIN11-	Isolated input #11 – Negative pole
13	IIN12+	Isolated input #12 – Positive pole
14	IIN13+	Isolated input #13 – Positive pole
15	IIN14+	Isolated input #14 – Positive pole

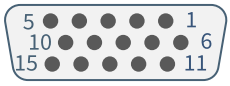
Pin	Signal	Usage
16	IOUT12+	Isolated contact output #12 – Positive pole
17	TTLIO12	TTL input/output #12
18	GND	Ground
19	DIN11-	High-speed differential input #11 – Negative pole
20	DIN11+	High-speed differential input #11 – Positive pole
21	IIN12-	Isolated input #12 – Negative pole
22	IOUT11-	Isolated contact output #11 – Negative pole
23	IOUT11+	Isolated contact output #11 – Positive pole
24	GND	Ground
25	TTLIO11	TTL input/output #11
26	+12V	+12 V Power output

External I/O Connector

Applies to:
MonoCXP12LH DuoCXP12

Connector description

Property	Value
Name	External I/O
Type	15-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	DIN12+	High-speed differential input #12 – Positive pole
2	IIN11+	Isolated input #11 – Positive pole
3	IIN12+	Isolated input #12 – Positive pole
4	TTLIO11	TTL input/output #11
5	GND	Ground
6	DIN11+	High-speed differential input #11 – Positive pole
7	DIN12-	High-speed differential input #12 – Negative pole
8	IIN12-	Isolated input #12 – Negative pole
9	IOUT11+	Isolated contact output #11 – Positive pole
10	GND	Ground
11	DIN11-	High-speed differential input #11 – Negative pole
12	IIN11-	Isolated input #11 – Negative pole
13	IOUT11-	Isolated contact output #11 – Negative pole
14	TTLIO12	TTL input/output #12
15	+12V	+12 V Power output

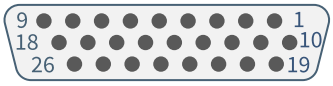
3610/3612 External I/O Connector

Applies to:

3610 3612

Connector description

Property	Value
Name	External I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	MIO03	Single-ended I/O #3 or differential I/O #3 positive pole
3	MIO05	Single-ended I/O #5 or differential I/O #5 positive pole
4	GND	Ground
5	MIO10-	Single-ended I/O #10 or differential I/O #9 negative pole
6	MIO14	Single-ended I/O #14 or differential I/O #13 negative pole
7	MIO18	Single-ended I/O #18 or differential I/O #17 negative pole
8	GND	Ground
9	MIO19	Single-ended I/O #19 or differential I/O #19 positive pole
10	GND	Ground
11	MIO04	Single-ended I/O #4 or differential I/O #3 negative pole
12	MIO06-	Single-ended I/O #6 or differential I/O #5 negative pole
13	MIO07	Single-ended I/O #7 or differential I/O #7 positive pole
14	GND	Ground
15	MIO09	Single-ended I/O #9 or differential I/O #9 positive pole

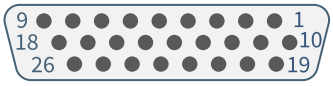
Pin	Signal	Usage
16	MIO13	Single-ended I/O #13 or differential I/O #13 positive pole
17	MIO17	Single-ended I/O #17 or differential I/O #17 positive pole
18	MIO20	Single-ended I/O #20 or differential I/O #19 negative pole
19	MIO02	Single-ended I/O #2 or differential I/O #1 negative pole
20	MIO01	Single-ended I/O #1 or differential I/O #1 positive pole
21	MIO08	Single-ended I/O #8 or differential I/O #7 negative pole
22	MIO12	Single-ended I/O #12 or differential I/O #11 negative pole
23	MIO11	Single-ended I/O #11 or differential I/O #11 positive pole
24	MIO16	Single-ended I/O #16 or differential I/O #15 negative pole
25	MIO15	Single-ended I/O #15 or differential I/O #15 positive pole
26	+12V	+12 V Power output

3614 External I/O 1 Connector

Applies to:
3614

Connector description

Property	Value
Name	External I/O 1
Type	26-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN12+	High-speed differential input #12 – Positive pole
3	IIN11+	Isolated input #11 – Positive pole
4	IIN13-	Isolated input #13 – Negative pole
5	IIN14-	Isolated input #14 – Negative pole
6	IOUT12-	Isolated contact output #12 – Negative pole
7	GND	Ground
8		Not connected
9	GND	Ground
10	GND	Ground
11	DIN12-	High-speed differential input #12 – Negative pole
12	IIN11-	Isolated input #11 – Negative pole
13	IIN12+	Isolated input #12 – Positive pole
14	IIN13+	Isolated input #13 – Positive pole
15	IIN14+	Isolated input #14 – Positive pole

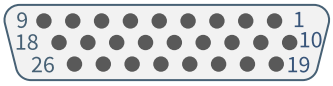
Pin	Signal	Usage
16	IOUT12+	Isolated contact output #12 – Positive pole
17	TTLIO12	TTL input/output #12
18	GND	Ground
19	DIN11-	High-speed differential input #11 – Negative pole
20	DIN11+	High-speed differential input #11 – Positive pole
21	IIN12-	Isolated input #12 – Negative pole
22	IOUT11-	Isolated contact output #11 – Negative pole
23	IOUT11+	Isolated contact output #11 – Positive pole
24	GND	Ground
25	TTLIO11	TTL input/output #11
26	+12V	+12 V Power output

3614 External I/O 2 Connector

Applies to:
3614

Connector description

Property	Value
Name	External I/O 2
Type	26-pin 3-row high-density female sub-D connector
Location	Card bracket
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN22+	High-speed differential input #22 – Positive pole
3	IIN21+	Isolated input #21 – Positive pole
4	IIN23-	Isolated input #23 – Negative pole
5	IIN24-	Isolated input #24 – Negative pole
6	IOUT22-	Isolated contact output #22 – Negative pole
7	GND	Ground
8		Not connected
9	GND	Ground
10	GND	Ground
11	DIN22-	High-speed differential input #22 – Negative pole
12	IIN21-	Isolated input #21 – Negative pole
13	IIN22+	Isolated input #22 – Positive pole
14	IIN23+	Isolated input #23 – Positive pole
15	IIN24+	Isolated input #24 – Positive pole

Pin	Signal	Usage
16	IOUT22+	Isolated contact output #22 – Positive pole
17	TTLIO22	TTL input/output #22
18	GND	Ground
19	DIN21-	High-speed differential input #21 – Negative pole
20	DIN21+	High-speed differential input #21 – Positive pole
21	IIN22-	Isolated input #22 – Negative pole
22	IOUT21-	Isolated contact output #21 – Negative pole
23	IOUT21+	Isolated contact output #21 – Positive pole
24	GND	Ground
25	TTLIO21	TTL input/output #21
26	+12V	+12 V Power output

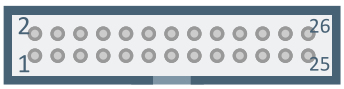
Internal I/O 1 Connector

Applies to:

Mono	Duo	Quad	QuadG3	QuadG3LH	QuadG3DF
Quad3DLLE	Octo	QuadCXP12	QuadCXP12J	MonoCXP12LH	DuoCXP12

Connector description

Property	Value
Name	Internal I/O 1
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN11+	High-speed differential input #11 – Positive pole
4	DIN11-	High-speed differential input #11 – Negative pole
5	DIN12+	High-speed differential input #12 – Positive pole
6	DIN12-	High-speed differential input #12 – Negative pole
7	IIN11+	Isolated input #11 – Positive pole
8	IIN11-	Isolated input #11 – Negative pole
9	IIN12+	Isolated input #12 – Positive pole
10	IIN12-	Isolated input #12 – Negative pole
11	IIN13+	Isolated input #13 – Positive pole
12	IIN13-	Isolated input #13 – Negative pole
13	IIN14+	Isolated input #14 – Positive pole
14	IIN14-	Isolated input #14 – Negative pole

Pin	Signal	Usage
15	IOUT11+	Isolated contact output #11 – Positive pole
16	IOUT11-	Isolated contact output #11 – Negative pole
17	IOUT12+	Isolated contact output #12 – Positive pole
18	IOUT12-	Isolated contact output #12 – Negative pole
19	TTLIO11	TTL input/output #11
20	GND	Ground
21	TTLIO12	TTL input/output #12
22	GND	Ground
23		Not connected
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

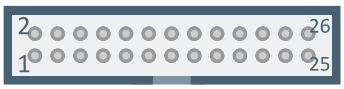
Internal I/O 2 Connector

Applies to:

Duo | Quad | QuadG3 | QuadG3LH | Quad3DLLE | QuadCXP12 | QuadCXP12J

Connector description

Property	Value
Name	Internal I/O 2
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN21+	High-speed differential input #21 – Positive pole
4	DIN21-	High-speed differential input #21 – Negative pole
5	DIN22+	High-speed differential input #22 – Positive pole
6	DIN22-	High-speed differential input #22 – Negative pole
7	IIN21+	Isolated input #21 – Positive pole
8	IIN21-	Isolated input #21 – Negative pole
9	IIN22+	Isolated input #22 – Positive pole
10	IIN22-	Isolated input #22 – Negative pole
11	IIN23+	Isolated input #23 – Positive pole
12	IIN23-	Isolated input #23 – Negative pole
13	IIN24+	Isolated input #24 – Positive pole
14	IIN24-	Isolated input #24 – Negative pole

Pin	Signal	Usage
15	IOUT21+	Isolated contact output #21 – Positive pole
16	IOUT21-	Isolated contact output #21 – Negative pole
17	IOUT22+	Isolated contact output #22 – Positive pole
18	IOUT22-	Isolated contact output #22 – Negative pole
19	TTLIO21	TTL input/output #21
20	GND	Ground
21	TTLIO22	TTL input/output #22
22	GND	Ground
23		Not connected
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

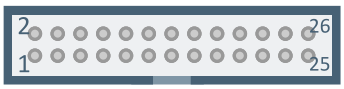
3610/3612 Internal I/O Connector

Applies to:

3610 3612

Connector description

Property	Value
Name	Internal I/O
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	MIO01	Single-ended I/O #1 or differential I/O #1 positive pole
4	MIO02	Single-ended I/O #2 or differential I/O #1 negative pole
5	MIO03	Single-ended I/O #3 or differential I/O #3 positive pole
6	MIO04	Single-ended I/O #4 or differential I/O #3 negative pole
7	MIO05	Single-ended I/O #5 or differential I/O #5 positive pole
8	MIO06	Single-ended I/O #6 or differential I/O #5 negative pole
9	MIO07	Single-ended I/O #7 or differential I/O #7 positive pole
10	MIO08	Single-ended I/O #8 or differential I/O #7 negative pole
11	GND	Ground
12	GND	Ground
13	MIO09	Single-ended I/O #9 or differential I/O #9 positive pole
14	MIO10	Single-ended I/O #10 or differential I/O #9 negative pole
15	MIO11	Single-ended I/O #11 or differential I/O #11 positive pole

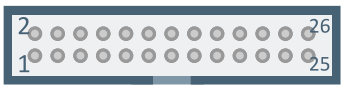
Pin	Signal	Usage
16	MIO12	Single-ended I/O #12 or differential I/O #11 negative pole
17	MIO13	Single-ended I/O #13 or differential I/O #13 positive pole
18	MIO14	Single-ended I/O #14 or differential I/O #13 negative pole
19	MIO15	Single-ended I/O #15 or differential I/O #15 positive pole
20	MIO16	Single-ended I/O #16 or differential I/O #15 negative pole
21	MIO17	Single-ended I/O #17 or differential I/O #17 positive pole
22	MIO18	Single-ended I/O #18 or differential I/O #17 negative pole
23	MIO19	Single-ended I/O #19 or differential I/O #19 positive pole
24	MIO20	Single-ended I/O #20 or differential I/O #19 negative pole
25	+12V	+12 V Power output
26	+12V_RTN	Ground

3614 Internal I/O 2 Connector

Applies to:
3614

Connector description

Property	Value
Name	Internal I/O 2
Type	26-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	GND	Ground
3	DIN21+	High-speed differential input #21 – Positive pole
4	DIN21-	High-speed differential input #21 – Negative pole
5	DIN22+	High-speed differential input #22 – Positive pole
6	DIN22-	High-speed differential input #22 – Negative pole
7	IIN21+	Isolated input #21 – Positive pole
8	IIN21-	Isolated input #21 – Negative pole
9	IIN22+	Isolated input #22 – Positive pole
10	IIN22-	Isolated input #22 – Negative pole
11	IIN23+	Isolated input #23 – Positive pole
12	IIN23-	Isolated input #23 – Negative pole
13	IIN24+	Isolated input #24 – Positive pole
14	IIN24-	Isolated input #24 – Negative pole
15	IOUT21+	Isolated contact output #21 – Positive pole

Pin	Signal	Usage
16	IOUT21-	Isolated contact output #21 – Negative pole
17	IOUT22+	Isolated contact output #22 – Positive pole
18	IOUT22-	Isolated contact output #22 – Negative pole
19	TTLIO21	TTL input/output #21
20	GND	Ground
21	TTLIO22	TTL input/output #22
22	GND	Ground
23		Not connected
24	GND	Ground
25	+12V	+12 V Power output
26	+12V_RTN	Ground

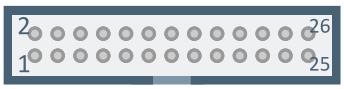
I/O Extension Connector

Applies to:

Octo | QuadCXP12 | QuadCXP12J | MonoCXP12LH | DuoCXP12

Connector description

Property	Value
Name	I/O Extension
Type	26-pin dual-row 0.050" pitch pin header with shrouding
Location	Printed circuit board
Usage	I/O extension cable socket



Pin assignments

Pin	Signal	Usage
1	IOEXT1WIRE	1-wire serial I/O
2	GND	Ground
3	IOEXT01	I/O Extension #1
4	+3V3	+3.3 V Power
5	IOEXT02	I/O Extension #2
6	GND	Ground
7	IOEXT03	I/O Extension #3
8	+3V3	+3.3 V Power
9	IOEXT04	I/O Extension #4
10	GND	Ground
11	IOEXT05	I/O Extension #5
12	+3V3	+3.3 V Power
13	IOEXT06	I/O Extension #6
14	GND	Ground
15	IOEXT07	I/O Extension #7

Pin	Signal	Usage
16	+3V3	+3.3 V Power
17	IOEXT08	I/O Extension #8
18	GND	Ground
19	IOEXT09	I/O Extension #9
20	12V	12V Power
21	IOEXT10	I/O Extension #10
22	GND	Ground
23	IOEXT11	I/O Extension #11
24	12V	12V Power
25	IOEXT12	I/O Extension #12
26	GND	Ground

C2C-Link Connector

Applies to:

Mono	Duo	Quad	QuadG3	QuadG3LH	QuadG3DF
Quad3DLLE	Octo	QuadCXP12	QuadCXP12J	MonoCXP12LH	DuoCXP12
1636					

Connector description

Property	Value
Name	C2C-Link
Type	6-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	Card-to-card link

Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	CSync1	Card-to-card synchronization bus – Signal 1
3	GND	Ground
4	CSync2	Card-to-card synchronization bus – Signal 2
5	GND	Ground
6	CSync3	Card-to-card synchronization bus – Signal 3

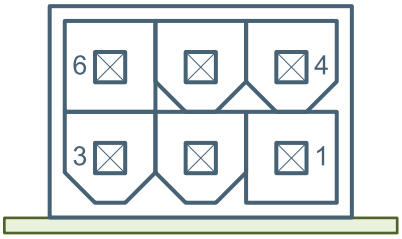
Auxiliary Power Input Connector

Applies to:

Mono	Duo	Quad	QuadG3	QuadG3LH	QuadG3DF
Quad3DLLE	Octo	QuadCXP12	QuadCXP12J	MonoCXP12LH	DuoCXP12

Connector description

Property	Value
Name	Auxiliary Power Input
Type	6-pin PCI Express x16 Graphics 150W ATX power socket connector
Location	Printed circuit board
Usage	DC power input for PoCXP and GPIO power output



Pin assignments

Pin	Signal	Usage
1	+12VIN	Auxiliary +12 V input
2	+12VIN	Auxiliary +12 V input
3	+12VIN	Auxiliary +12 V input
4	GND	Ground
5	SenseIN	Power source presence detection
6	GND	Ground

2.3. LEDs

CoaXPress LED lamps

Each connector of the CoaXPress Host Interface is associated with a LED lamp mounted on the bracket (for PCie cards only).

LED lamps mode control

The LampMode feature of the Interface module defines the lamps operation mode:

- When set to Standard (default value), the lamps indicate the state of the CoaXPress Link connection.
- When set to Dark, all lamps are turned off.
- When set to Error, all lamps are turned off unless error conditions are detected.
- When set to Custom, all lamps are controlled by LampCustomValue, a bitfield where each bit is mapped onto a lamp with 1 for orange and 0 for off by the LampCustomLedA … LampCustomLedH boolean features.

CoaXPress Host Indicator LED lamps states

States description

Symbol	Indication	State
	Off	No power
	Solid orange	System booting
	AlternateFlash_12_5 green / orange[1]	Connection detection in progress; PoCXP active
	Flash_12_5 orange[2]	Connection detection in progress; PoCXP not in use
	AlternateFlash_0_5 red / green	Device/ Host incompatible; PoCXP active
	AlternateFlash_0_5 red / orange	Device/ Host incompatible; PoCXP not in use

[1]Shown for a minimum of 1 second even if the connection detection is faster

[2]Shown for a minimum of 1 second even if the connection detection is faster

Symbol	Indication	State
	Solid red	PoCXP over-current
	Solid green	Device / Host connected, but no data being transferred
	Flash_1 orange	Device / Host connected, waiting for event (e.g. trigger, exposure pulse)
	Flash_12_5 green	Device / Host connected, data being transferred
	500 ms red pulse[1]	Error during data transfer (e.g. CRC error, single bit error detected)
	AlternateFlash_0_5 green / orange	Connection test packets being sent
	Flash_12_5 red	System error (e.g. internal error)

Flashing states timing definitions

Indication	Frequency	Duty Cycle
Flash_12_5	12.5 Hz	25% (20 milliseconds on, 60 milliseconds off)
Flash_1	1 Hz	20% (200 milliseconds on, 800 milliseconds off)
Flash_0_5	0.5 Hz	50% (1 second on, 1 second off)
AlternateFlash_12_5	12.5 Hz	25% (20 milliseconds on color 1, 60 milliseconds off, 20 milliseconds on color 2, 60 milliseconds off)
AlternateFlash_0_5	0.5 Hz	50% (1 second on color 1, 1 second off, 1 second on color 2, 1 second off)

[1]In case of multiple errors, there shall be at least two green Flash_12_5 pulses before the next error is indicated

Board Status LED

Board status LED indicator states

LED state	Symbol	Meaning
Off		**No power.** The board is not powered or the power distribution network is not functional.
Solid green		**Board status OK.** The main power distribution network is operational and the FPGA start-up procedure has successfully completed.
Solid red		**Board status NOK.** Possible causes are: • There is no power delivered on the +12 V rail of the PCI Express connector slot • The FPGA start-up procedure is not completed. *The normal completion time is around 100 milliseconds.* • At least one power converter of the main power distribution network is unable to operate properly. *This might be caused by excessive temperature due to inadequate board cooling, accidental short-circuits having blown one (or more) protection fuses, inappropriate supply voltages, etc.*

FPGA Status LED

FPGA status LED indicator states

LED state	Symbol	Meaning
Off		**Board not powered.**
Solid green		**FPGA status OK.** All the FPGA clock networks and the DDR memory are operating normally.
Solid red		**FPGA status NOK.** Possible causes are: • At least one FPGA clock network is not operating normally. *This might be caused by excessive jitter on external clock signals of the CoaXPress or the PCI Express interfaces.* • The DDR memory controller has not been able to successfully perform the calibration procedure.

2.4. Firmware Recovery Switch

Introduction

The firmware recovery switch is implemented with a 3-pin 1-row header and a jumper. The jumper has two positions: *normal* and *recovery*.

Normal position

At the next power ON, the latest firmware successfully written into the Flash EEPROM is used to program the FPGA.

After FPGA startup completion, the card exhibits the standard PCI ID and the Coaxlink driver allows normal operation.

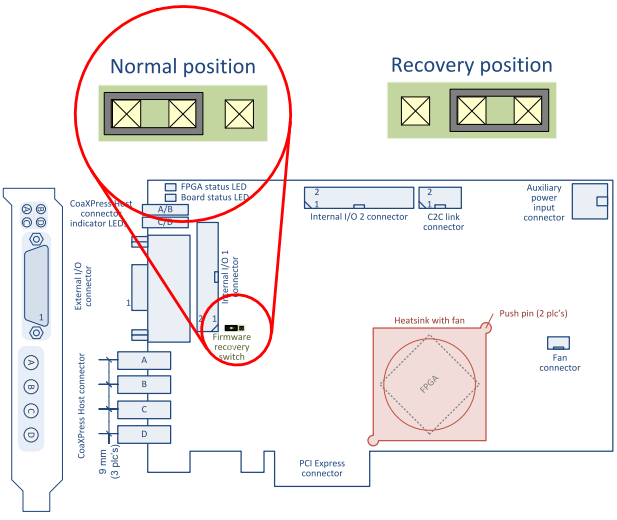
This is the factory default jumper position.

Recovery position

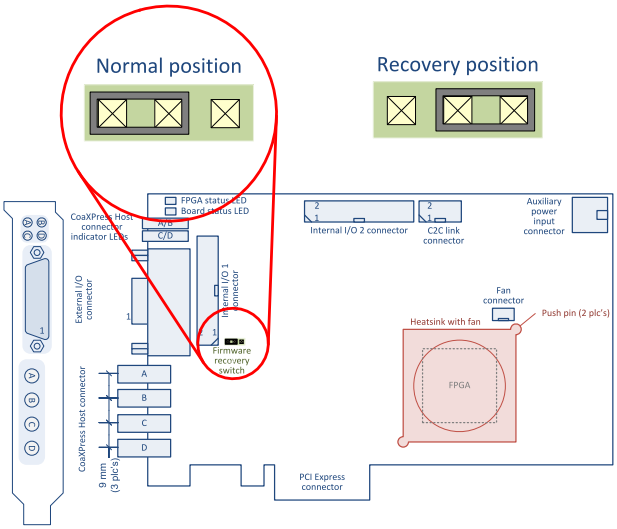
At the next power ON, the last but one firmware successfully written into the Flash EEPROM is used to program the FPGA.

After FPGA startup completion, the card exhibits the recovery PCI ID and the Coaxlink driver inhibits image acquisition.

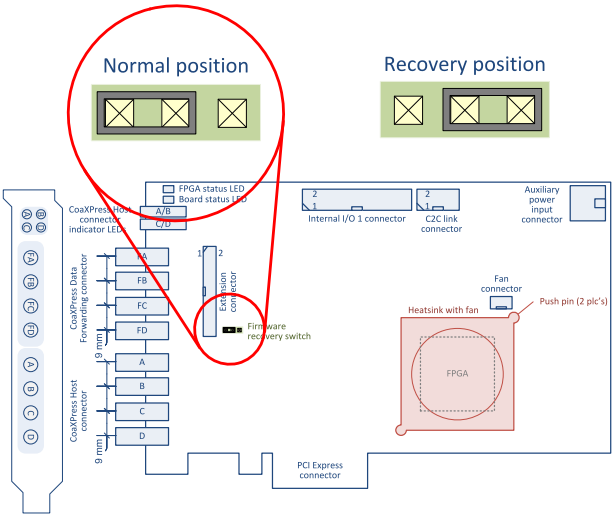
1632 Coaxlink Quad



1633 Coaxlink Quad G3, 1633-LH Coaxlink Quad G3 LH, 1637 Coaxlink Quad 3D-LLE



1635 Coaxlink Quad G3 DF, 3601 Coaxlink CoaXPress Simulator



NOTE
The normal position of the jumper (i.e. bracket side) is common to all Coaxlink PCI Express cards.

2.5. Physical Characteristics

Dimensions and weight

Product	Length	Width	Weight
1630 Coaxlink Mono	167.65 mm, 6.6 in	111.15 mm, 4.38 in	150 g, 5.29 oz
1631 Coaxlink Duo	167.65 mm, 6.6 in	111.15 mm, 4.38 in	160 g, 5.64 oz
1632 Coaxlink Quad	167.65 mm, 6.6 in	111.15 mm, 4.38 in	170 g, 6.00 oz
1633 Coaxlink Quad G3	167.65 mm, 6.6 in	111.15 mm, 4.38 in	180 g, 6.35 oz
1633-LH Coaxlink Quad G3 LH	167.65 mm, 6.6 in	111.15 mm, 4.38 in	265 g, 9.35 oz
1635 Coaxlink Quad G3 DF	167.65 mm, 6.6 in	111.15 mm, 4.38 in	186 g, 6.56 oz
1637 Coaxlink Quad 3D-LLE	167.65 mm, 6.6 in	111.15 mm, 4.38 in	180 g, 6.35 oz
3602 Coaxlink Octo	167.65 mm, 6.6 in	111.15 mm, 4.38 in	189 g, 6.67 oz
3603 Coaxlink Quad CXP-12	167.65 mm, 6.6 in	111.15 mm, 4.38 in	196 g, 6.91 oz
3620 Coaxlink Quad CXP-12 JPEG	167.65 mm, 6.6 in	111.15 mm, 4.38 in	196 g, 6.91 oz
3621-LH Coaxlink Mono CXP-12 LH	167.65 mm, 6.6 in	68.90 mm, 2.71 in	160 g, 5.64 oz
3622 Coaxlink Duo CXP-12	167.65 mm, 6.6 in	68.90 mm, 2.71 in	125 g, 4.40 oz

3. Electrical Specification

Electrical specification of the product(s) including: electrical characteristics of all the input/output ports, description of the power distribution, power requirements, etc.

3.1. CoaXPress Host Interface

Electrical specification of the CoaXPress Host interface

CoaXPress Host Interface Type per Product

Each connection of the CoaXPress Host interface implements a *Host Transceiver* (HT) and a *Power Transmitting Unit* (PTU).

Product	HT Type
1630 Coaxlink Mono	"CXP-6 Host Transceiver" on page 63
1631 Coaxlink Duo	"CXP-6 Host Transceiver" on page 63
1632 Coaxlink Quad	"CXP-6 Host Transceiver" on page 63
1633 Coaxlink Quad G3	"CXP-6 Host Transceiver" on page 63
1633-LH Coaxlink Quad G3 LH	"CXP-6 Host Transceiver" on page 63
1635 Coaxlink Quad G3 DF	"CXP-6 Host Transceiver" on page 63
1637 Coaxlink Quad 3D-LLE	"CXP-6 Host Transceiver" on page 63
3602 Coaxlink Octo	"CXP-6 Host Transceiver" on page 63
3603 Coaxlink Quad CXP-12	"CXP-12 Host Transceiver" on the next page
3620 Coaxlink Quad CXP-12 JPEG	"CXP-12 Host Transceiver" on the next page
3621-LH Coaxlink Mono CXP-12 LH	"CXP-12 Host Transceiver" on the next page
3622 Coaxlink Duo CXP-12	"CXP-12 Host Transceiver" on the next page

CXP-12 Host Transceiver

Applies to:
QuadCXP12 | QuadCXP12J | MonoCXP12LH | DuoCXP12

The Host transceiver implements a *high-speed cable receiver* and a *low-speed cable driver* for *CXP-12* speeds.

It fulfills the electrical specification of the CoaXPress 2.0 standard. Namely:

- The cable receiver requirements for the high-speed connection described in Table 2 of the Annex B of the CoaXPress Standard Version 2.0
- The cable driver requirements for the low-speed connection described in Table 3 of the Annex B of the CoaXPress Standard Version 2.0

Host Transceiver Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
High-speed connection bit rate		1.25		12.50	GT/s
Low-speed connection bit rate	1.25 GT/s up to 6.25 GT/s		20.833		MT/s
	10.0 GT/s and 12.5 GT/S		41.666		MT/s
Max. cable length	BELDEN 1694 @ 1.25 GT/s	130			m
	BELDEN 1694 @ 2.5 GT/s	115			m
	BELDEN 1694 @ 3.125 GT/s	100			m
	BELDEN 1694 @ 5 GT/s	80			m
	BELDEN 1694 @ 6.25 GT/s	70			m
	BELDEN 1694 @ 10.0 GT/s	50			m
	BELDEN 1694 @12.5GT/s	40			m

CXP-6 Host Transceiver

Applies to:

Mono | Duo | Quad | QuadG3 | QuadG3LH | QuadG3DF | Quad3DLLE | Octo

The Host transceiver implements a *high-speed cable receiver* and a *low-speed cable driver* for *CXP-6* speeds.

It fulfills the electrical specification of the CoaXPress 1.1 standard. Namely:

- The cable receiver requirements for the high-speed connection described in Table 2 of the Annex B of the CoaXPress Standard 1.1
- The cable driver requirements for the low-speed connection described in Table 3 of the Annex B of the CoaXPress Standard 1.1

Host Transceiver Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
High-speed connection bit rate		1.25		6.25	GT/s
Low-speed connection bit rate			20.833		MT/s
Max. cable length	BELDEN 1694 @ 1.25 GT/s	130			m
	BELDEN 1694 @ 2.5 GT/s	110			m
	BELDEN 1694 @ 3.125 GT/s	100			m
	BELDEN 1694 @ 5 GT/s	60			m
	BELDEN 1694 @ 6.25 GT/s	40			m

Power Transmitting Unit

The Power Transmitting Unit provides 17 W* of 24 V DC power per connection, over-current protection (OCP) and PoCXP device detection as specified by the CoaXPress Standard.

Power Transmitting Unit Specification

Parameter	Min.	Typ.	Max.	Unit
DC output voltage	22	24	26	V
Available output power	17*			W
OCP holding current	790			mA
OCP nominal trip current			5	A
Device detection sense resistance		4.7		kΩ

NOTE
(*) 25 W for **3621-LH Coaxlink Mono CXP-12 LH**

NOTE
The above specification applies over the whole operating temperature range of the Coaxlink card.

See also: Refer to Power Over CoaXPress in the Functional Guide

3.2. PCI Express Interface

Specification of the PCI Express Interface

The PCI Express Interface implements a *PCIe end-point* interface and provides *electrical power* to the Coaxlink card.

PCI Express end-point type per product

Product	Type
1630 Coaxlink Mono	"4-lane Rev 2.0 PCIe end-point" on page 68
1631 Coaxlink Duo	"4-lane Rev 2.0 PCIe end-point" on page 68
1632 Coaxlink Quad	"4-lane Rev 2.0 PCIe end-point" on page 68
1633 Coaxlink Quad G3	"4-lane Rev 3.0 PCIe end-point " on page 67
1633-LH Coaxlink Quad G3 LH	"4-lane Rev 3.0 PCIe end-point " on page 67
1635 Coaxlink Quad G3 DF	"4-lane Rev 3.0 PCIe end-point " on page 67
1637 Coaxlink Quad 3D-LLE	"4-lane Rev 2.0 PCIe end-point" on page 68
3602 Coaxlink Octo	"8-lane Rev 3.0 PCIe end-point" on the next page
3603 Coaxlink Quad CXP-12	"8-lane Rev 3.0 PCIe end-point" on the next page
3620 Coaxlink Quad CXP-12 JPEG	"8-lane Rev 3.0 PCIe end-point" on the next page
3621-LH Coaxlink Mono CXP-12 LH	"4-lane Rev 3.0 PCIe end-point " on page 67
3622 Coaxlink Duo CXP-12	"4-lane Rev 3.0 PCIe end-point " on page 67

8-lane Rev 3.0 PCIe end-point

Applies to:

Octo | QuadCXP12 | QuadCXP12J

The 8-lane Rev 3.0 PCIe end-point:

- complies with Revision 3.0 of the PCI Express Card Electromechanical specification.
- supports 1-lane, 2-lane, 4-lane and 8-lane link width
- supports PCIe Rev 3.0 link speed (8.0 GT/s with 128b/130b coding)
- supports PCIe Rev 2.0 link speed (5.0 GT/s with 8b/10b coding)
- supports the PCIe Rev 1.0 link speed (2.5 GT/s with 8b/10b coding)
- supports payload size up to 512 bytes
- offers the optimal performance when it is configured for 8-lane PCIe Rev 3.0 link speed (8 GT/s)

8-lane Rev 3.0 PCIe end-point to PC memory data transfer performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	8-lane @ 8 GT/s (PCIe Rev 3.0)		6,700		MB/s
	8-lane @ 5 GT/s (PCIe Rev 2.0)		3,400		MB/s
	4-lane @ 8 GT/s (PCIe Rev 3.0)		3,350		MB/s
	4-lane @ 5 GT/s (PCIe Rev 2.0)		1,700		MB/s
	2-lane @ 8 GT/s (PCIe Rev 3.0)		1,700		MB/s
	2-lane @ 5 GT/s (PCIe Rev 2.0)		800		MB/s
	1-lane @ 8 GT/s (PCIe Rev 3.0)		800		MB/s

4-lane Rev 3.0 PCIe end-point

Applies to:

QuadG3 | QuadG3LH | QuadG3DF | MonoCXP12LH | DuoCXP12

The 4-lane Rev 3.0 PCIe end-point:

- complies with Revision 3.0 of the PCI Express Card Electromechanical specification.
- supports 1-lane, 2-lane, and 4-lane link width
- supports PCIe Rev 3.0 link speed (8.0 GT/s with 128b/130b coding)
- supports PCIe Rev 2.0 link speed (5.0 GT/s with 8b/10b coding)
- *doesn't support* the PCIe Rev 1.0 link speed (2.5 GT/s with 8b/10b coding)
- supports payload size up to 512 bytes
- offers the optimal performance when it is configured for 4-lane PCIe Rev 3.0 link speed (8 GT/s)

4-lane Rev 3.0 PCIe end-point to PC memory data transfer performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	4-lane @ 8 GT/s (PCIe Rev 3.0)		3,350		MB/s
	4-lane @ 5 GT/s (PCIe Rev 2.0)		1,700		MB/s
	2-lane @ 8 GT/s (PCIe Rev 3.0)		1,700		MB/s
	2-lane @ 5 GT/s (PCIe Rev 2.0)		800		MB/s
	1-lane @ 8 GT/s (PCIe Rev 3.0)		800		MB/s

4-lane Rev 2.0 PCIe end-point

Applies to:

Mono | Duo | Quad | Quad3DLLE

The 4-lane Rev 2.0 PCIe end-point:

- complies with Revision 2.0 of the PCI Express Card Electromechanical specification.
- supports 1-lane, 2-lane, and 4-lane link width
- supports PCIe Rev 2.0 link speed (5.0 GT/s with 8b/10b coding)
- supports PCIe Rev 1.0 link speed (2.5 GT/s with 8b/10b coding)
- supports payload size up to 512 bytes
- offers the optimal performance when it is configured for 4-lane PCIe Rev 2.0 link speed (5 GT/s)

4-lane Rev 3.0 PCIe end-point to PC memory data transfer performance

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	4-lane @ 5 GT/s (PCIe Rev 2.0)		1,700		MB/s
	4-lane @ 2.5 GT/s (PCIe Rev 1.0)		800		MB/s
	2-lane @ 5 GT/s (PCIe Rev 2.0)		800		MB/s

3.3. Power Distribution

Introduction

The power distribution of a Coaxlink PCIe product has two distinct distribution networks:

- The main power distribution network
- The auxiliary power distribution network

Main power distribution network

The main power distribution network delivers power to *all the on-board electronic devices* including FPGA, memory chips, CoaXPress transceivers, I/O drivers and receivers, fan motor.

The network is fed by the Host PC motherboard through the +3.3 V and the +12 V power rails of the PCI Express slot connector. Protection fuses inserted at the input side of each power rail prevent potential fire hazards.

The *board status LED* reflects the global status of all the power converters of the main distribution network.

Auxiliary power distribution network

The auxiliary power distribution network delivers power to the external devices including:

- CoaXPress cameras using the PoCXP capability available on all connections of the CoaXPress Host connector
- System devices using the +12 V power output available on all I/O connectors

The network is fed by a 12 V external power supply attached to the auxiliary power input connector using a power cable terminated by a 6-pin PEG plug connector. A protection fuse inserted at the input side prevents potential fire hazards.

A 24-volt DC power converter provides power to each camera connection through a PoCXP transmitter unit. Each PoCXP transmitter unit implements an electronic fuse/switch that prevents potential fire hazards.

The +12 V power is distributed to all the I/O connectors through a common electronic fuse that prevents potential fire hazards.

The "CoaXPress LED lamps" on page 53 reflect the state of each CoaXPress host connection.

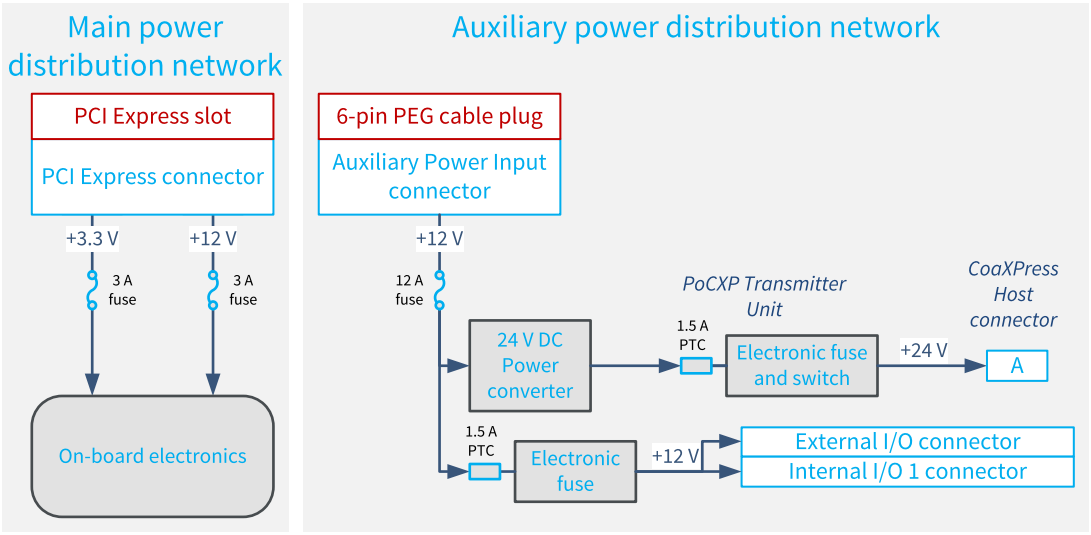
The following GenICam features of the Interface module report the status of the auxiliary power distribution network:

- AuxiliaryPowerInput reports the status of the auxiliary power input cable connection.
- AuxiliaryPower12VInput reports the status of the "12V Auxiliary Power Input" measured after the input fuse.
- CxpPoCxpPowerInputStatus reports the status of the 24 V power converter delivering power to all the PoCXP transmitter units.
- CxpPoCxpCurrent reports the current delivered by the PoCXP transmitter unit designated by CxpPoCxpHostConnectionSelector.
- CxpPoCxpVoltage reports the output voltage delivered by the PoCXP transmitter unit designated by CxpPoCxpHostConnectionSelector.

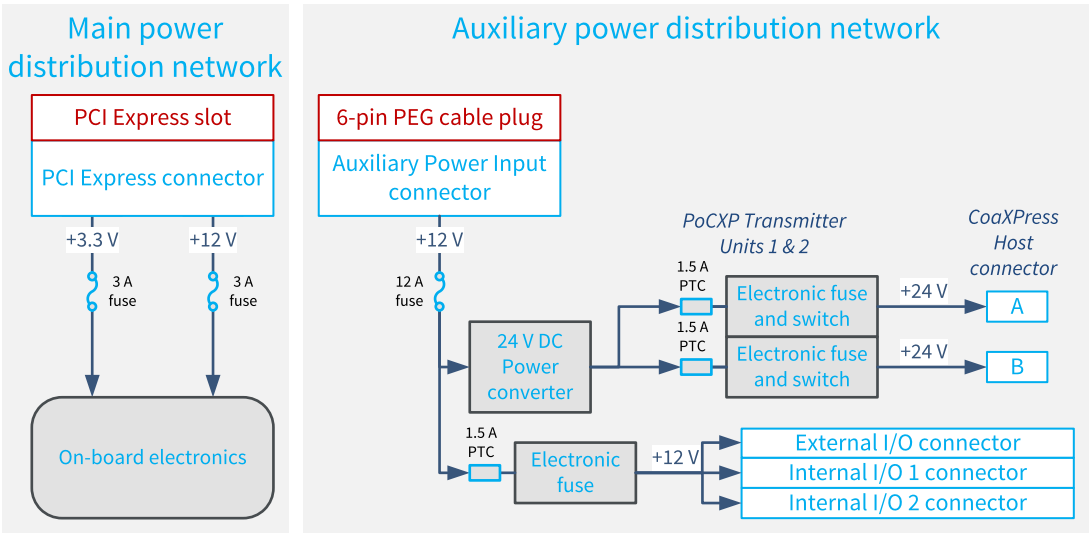
NOTE
The Coaxlink card can be operated without applying power to the auxiliary power distribution network.

Power distribution schemes per product

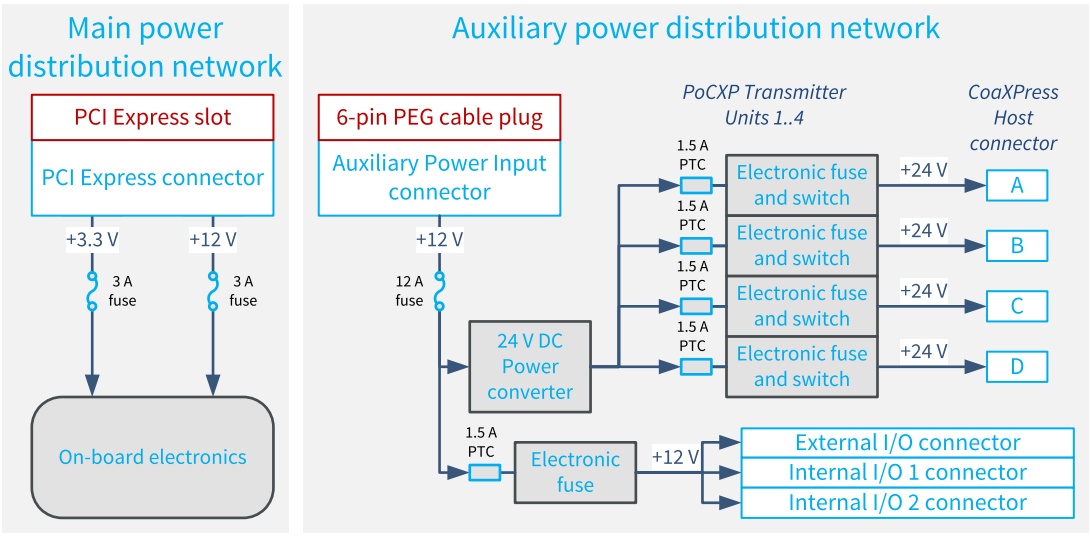
1630 Coaxlink Mono power distribution scheme



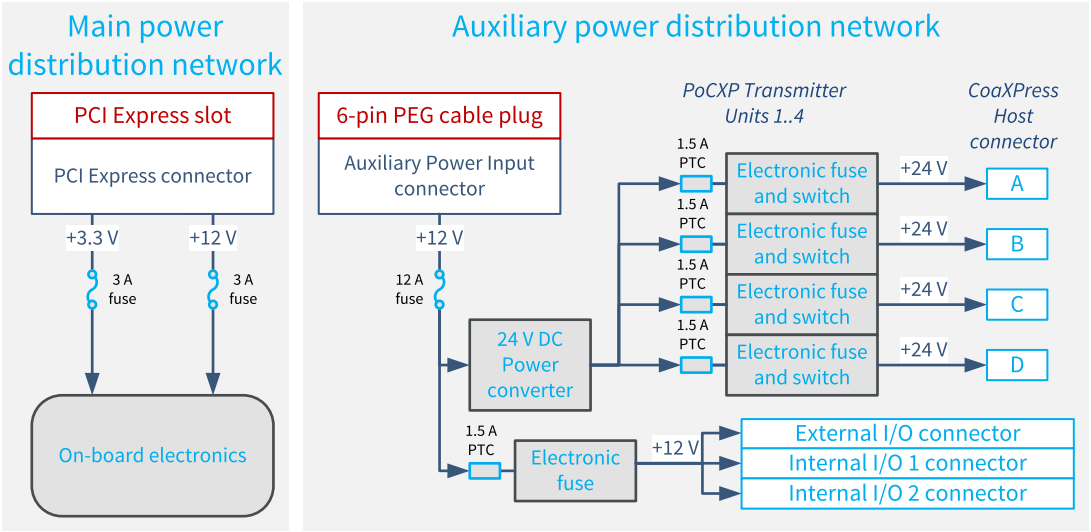
1631 Coaxlink Duo power distribution scheme



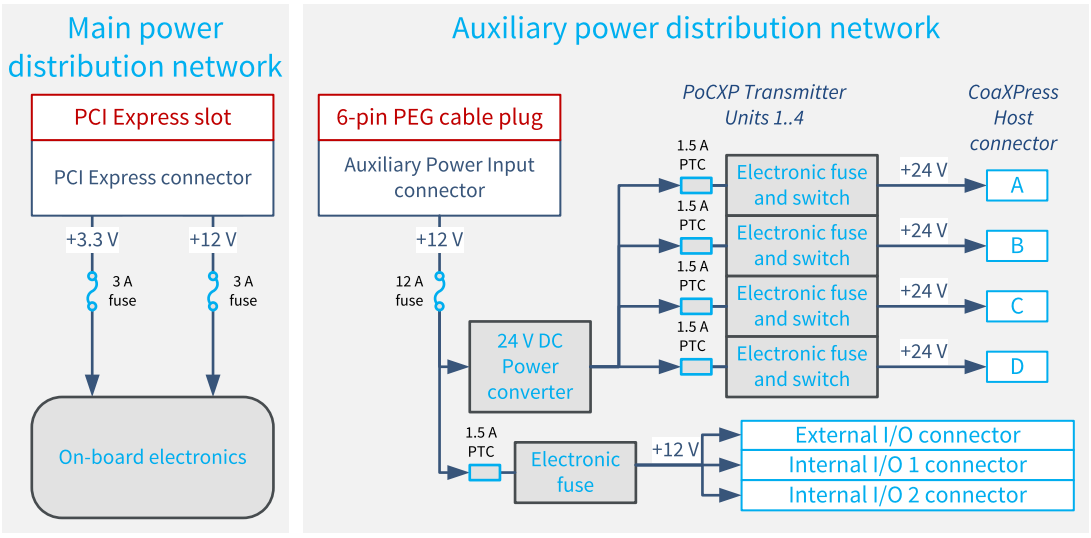
1632 Coaxlink Quad power distribution scheme



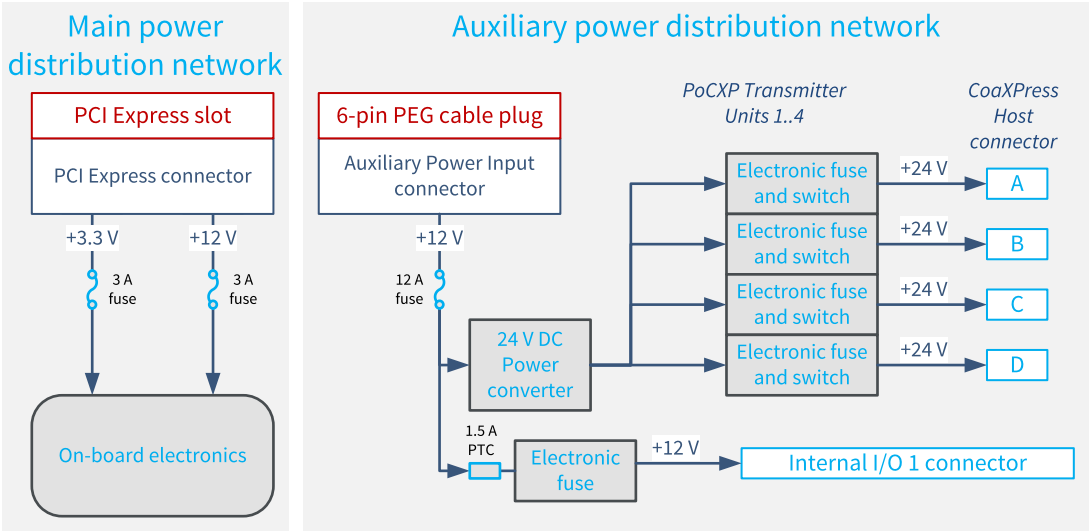
1633 Coaxlink Quad G3 power distribution scheme



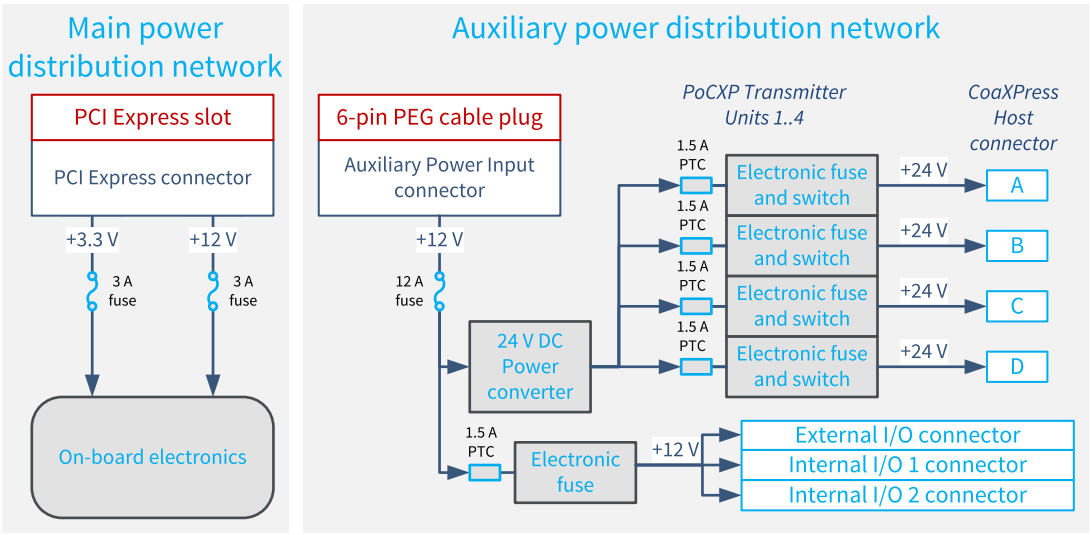
1633-LH Coaxlink Quad G3 LH power distribution scheme



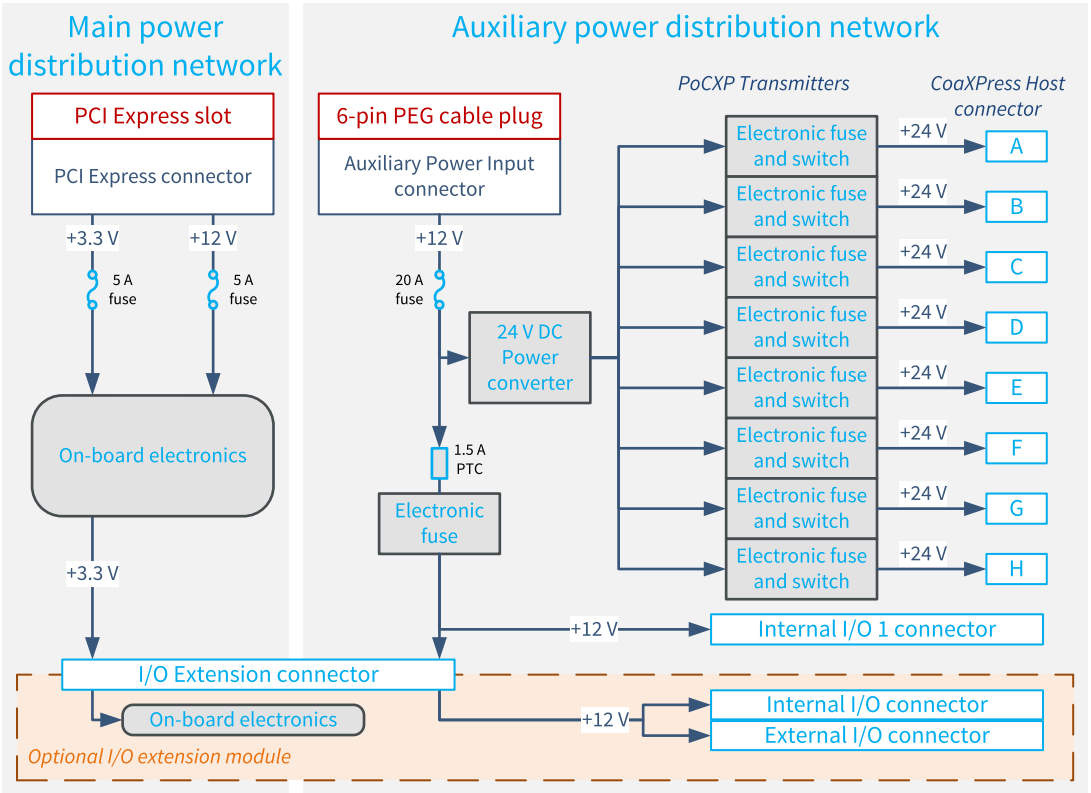
1635 Coaxlink Quad G3 DF power distribution scheme



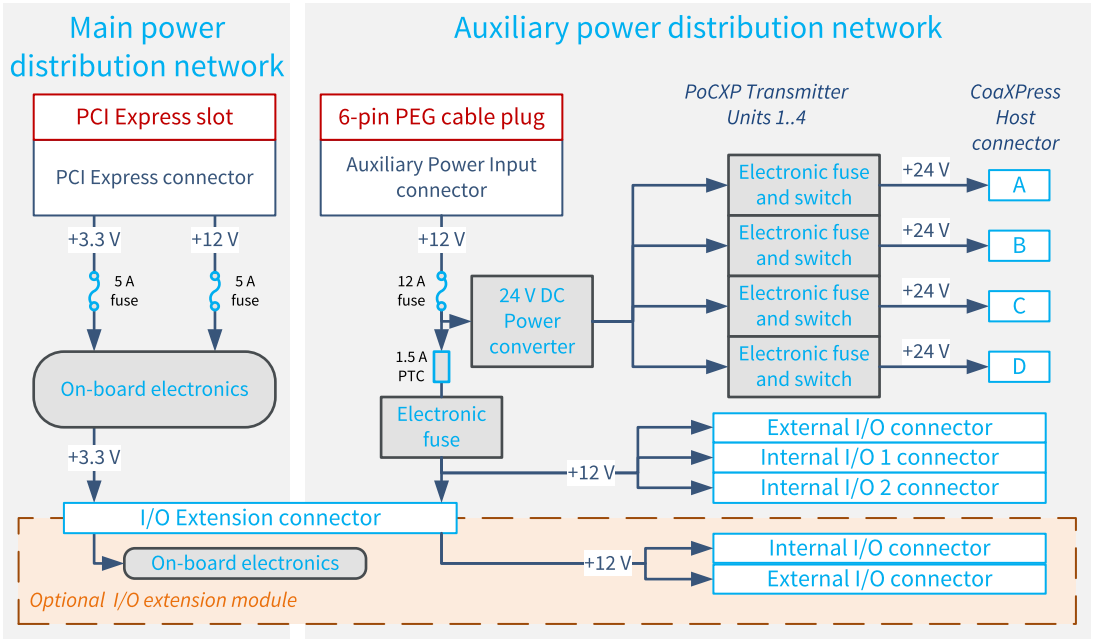
1637 Coaxlink Quad 3D-LLE power distribution scheme



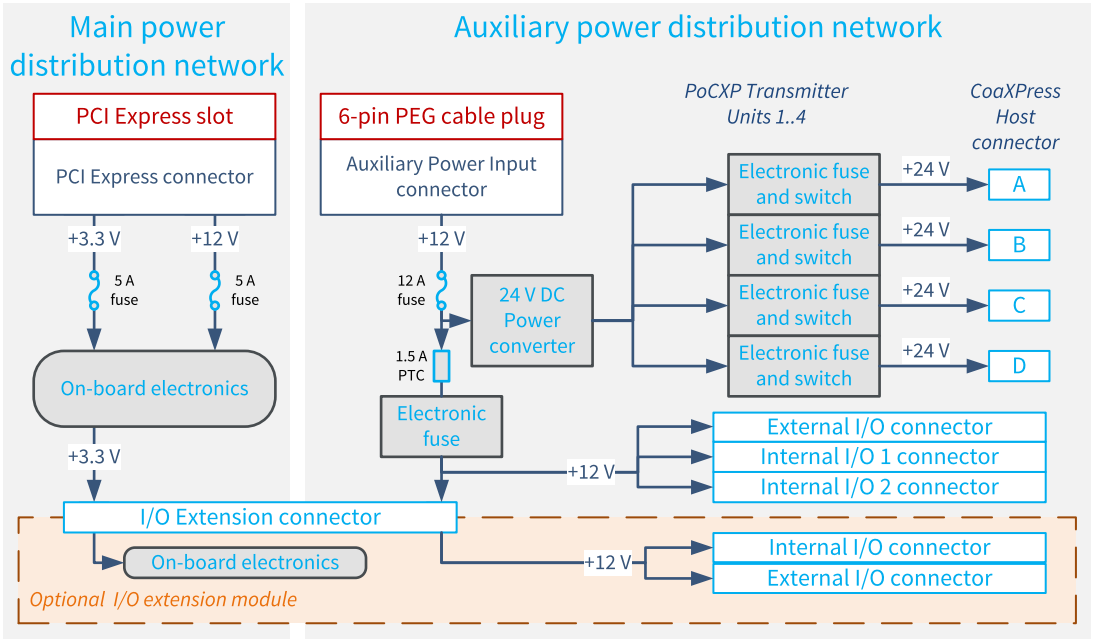
3602 Coaxlink Octo power distribution scheme



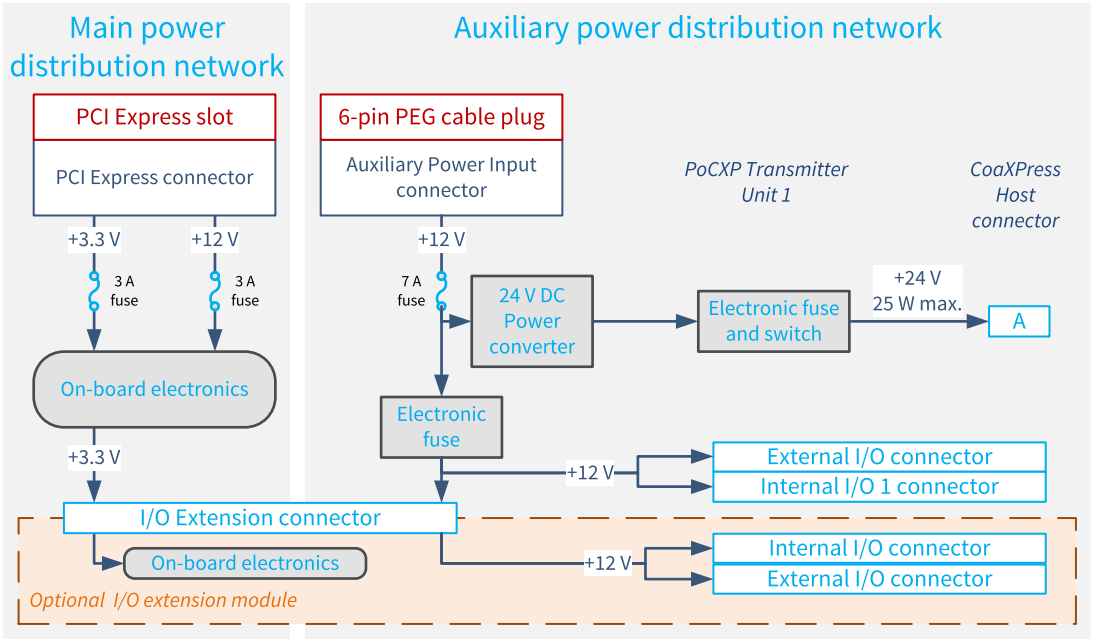
3603 Coaxlink Quad CXP-12 power distribution scheme



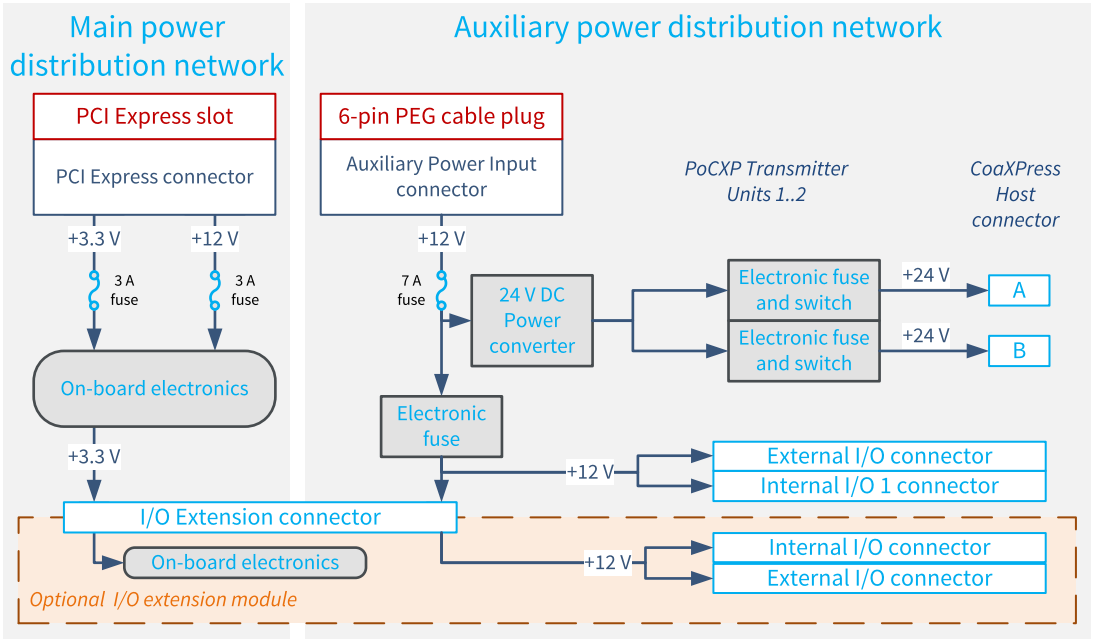
3620 Coaxlink Quad CXP-12 JPEG power distribution scheme



3621-LH Coaxlink Mono CXP-12 LH power distribution scheme



3622 Coaxlink Duo CXP-12 power distribution scheme



NOTE

- The fuses are not serviceable! When blown, the card must be returned to the factory.
- Electronic fuses are self-resettable fuses.

3.4. PCI Express Power

Power requirements per product

The following table provides the typical PCI Express power consumption for each product when it operates under the following conditions:

- Acquiring image data using all CoaXPress Host Interface connections operating at their maximum speed
- Delivering image data on the PCI Express configured for the largest link width and the highest link speed
- Operating @25°C [77 °F] ambient temperature and nominal supply voltages

Product	+12 V	+3.3 V	Total	Units
1630 Coaxlink Mono	7.2	2.1	9.3	W
1631 Coaxlink Duo	8.7	2.7	11.4	W
1632 Coaxlink Quad	9.6	2.5	12.1	W
1633 Coaxlink Quad G3	13	3.8	16.8	W
1633-LH Coaxlink Quad G3 LH	13	3.8	16.8	W
1635 Coaxlink Quad G3 DF	13	3.8	16.8	W
1637 Coaxlink Quad 3D-LLE	13	3.8	16.8	W
3602 Coaxlink Octo	11.8	4.2	16	W
3603 Coaxlink Quad CXP-12	9.8	7.3	17.1	W
3620 Coaxlink Quad CXP-12 JPEG	11.8	6.3	18.1	W
3621-LH Coaxlink Mono CXP-12 LH	8.5	3	11.5	W
3622 Coaxlink Duo CXP-12	10.5	4.3	14.8	W

Voltage requirements

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V

3.5. Auxiliary Power

Applies to PCI Express products only!

PCIe products with one PoCXP

Applies to:
Mono

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12 W I/O output power	0		12	W
DC input power for PoCXP	17 W PoCXP output power			19	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

Applies to:
MonoCXP12LH

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12 W I/O output power	0		12	W
DC input power for PoCXP	25 W PoCXP output power			19	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

PCIe products with two POCXP

Applies to:
Duo DuoCXP12

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12 W I/O output power	0		12	W
DC input power for PoCXP	34 W total PoCXP output power			37	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

PCIe products with four PoCXP

Applies to:

Quad | QuadG3 | QuadG3LH | QuadG3DF | Quad3DLLE | QuadCXP12 | QuadCXP12J

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12 W I/O output power	0		12	W
DC input power for PoCXP	68 W total PoCXP output power			74	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

PCIe products with eight PoCXP

Applies to:

Octo

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		11	12	13	V
DC input power for I/O	12 W I/O output power	0		12	W
DC input power for PoCXP	136 W total PoCXP output power			148	W
PoCXP output voltage		23	24	25	V
Power conversion efficiency		92.5			%

NOTE
The sense input of the PEG connector is intended for power source cable presence detection. It should be grounded at the power supply level.

NOTE
The power rating of the power source is application dependent.

3.6. I/O Power Output

Specification of the +12 V power output of the I/O connector

A non-isolated +12 V power output is available on every I/O connector.

The power originates from an external 12 V power supply plugged into the Auxiliary Power Input connector. It is distributed from a common electronic fuse to all the I/O connectors.

The electronic fuse provides the following protections:

- Limits the inrush current during power on sequence
- Protects the Coaxlink card and the power source against overload
- Protects the Coaxlink card the power source against short-circuits.

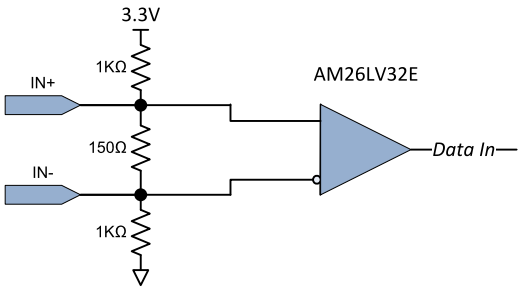
The sum of the load currents drawn from all the 12 V outputs of the I/O connectors must be lower or equal to the specified maximum output current.

I/O +12 V power output specification

Parameter	Conditions	Min.	Typ.	Max.	Units
Aggregated output current	Operating temperature range			1.0	A
Voltage drop across the electronic fuse	Max. output current			0.2	V

NOTE
The above specification applies over the whole operating temperature range of the Coaxlink card.

3.7. Differential Input



Differential Input Simplified Schematic

The receiver complies with the ANSI/TIA/EIA-422B specification.

DC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Common mode voltage		-7		+7	V
Differential sensitivity				200	mV
Input impedance			120		Ohm
ESD protection	Human Body Model (HBM)	15			kV
	Contact discharge	8			kV
	Air gap discharge	15			kV

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	100			ns
Pulse rate	0		5	MHz
10%-90% rise/fall time			1	µs

Logical map

The state of the port is reported as follows:

Relative V+/V- voltage	Logical State
V+ > V-	HIGH
V+ < V-	LOW
Unconnected input	HIGH

Compatible drivers

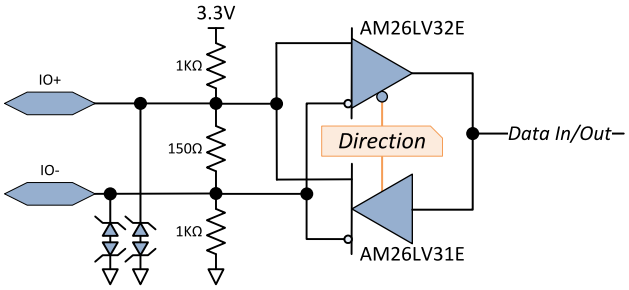
The following drivers are compatible with the high-speed differential input ports:

- RS-422/RS-485 differential line drivers
- Complementary TTL drivers

3.8. Differential Input/Output

Applies to:

3610 3612



Differential Input/Output Simplified Schematic

The driver and the receiver complies with the ANSI/TIA/EIA-422B specification.

DC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Common mode voltage		-7		+7	V
Input impedance			120		Ohm
ESD protection	Human Body Model (HBM)	15			kV
	Contact discharge	8			kV
	Air gap discharge	15			kV

Driver

Parameter	Conditions	Min.	Typ.	Max.	Units
Low-level output current				30	mA
Low-level output voltage	20 mA		0.2	0.4	V
High-level output current				-30	mA
High-level output voltage	-20 mA	2.4	3		V
Differential output voltage	0 mA	2		4	V

Receiver

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential amplitude		200			mV

AC characteristics

Driver

Parameter	Min.	Typ.	Max.	Units
Pulse width	50			ns
Pulse rate	0		10	MHz
10%-90% rise/fall time		TBD		µs

Receiver

Parameter	Min.	Typ.	Max.	Units
Pulse width	50			ns
Pulse rate	0		10	MHz
10%-90% rise/fall time		TBD		µs

Logical map

The state of the port is as follows:

Relative V+/V- voltage	Logical State
V+ > V-	HIGH
V+ < V-	LOW

Compatible sources

Sources with the following drivers are compatible:

- RS-422 differential line drivers
- Complementary TTL drivers

Compatible loads

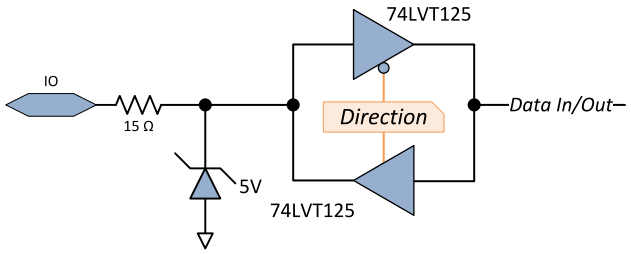
Loads with the following receivers are compatible:

- RS-422 differential line receivers

3.9. TTL Input/Output (Version 1)

Applies to:

Mono	Duo	Quad	QuadG3	QuadG3DF	Quad3DLLE
3614					



TTL Input/Output Simplified schematic

The port implements a 3.3 V LVTTL driver and a 5 V-compliant 3.3 V LVTTL receiver.

DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
ESD protection	Human Body Model (HBM)	2			kV

NOTE
The I/O port includes a latch-up protection.

Driver

Parameter	Conditions	Min.	Typ.	Max.	Units
Low-level output current				64	mA
Low-level output voltage	@ 8 mA		0.34	0.36	V
	@ 16 mA		0.48	0.55	V
	@ 32 mA		0.78	0.81	V
	@ 64 mA		1.34	1.36	V
High-level output current				-32	mA
High-level output voltage	@-8 mA; (1)	2.60	3.00		V
	@-16 mA; (1)	2.20	2.70		V
	@-32 mA; (1)	1.75	2.20		V
ESD protection	Human Body Model (HBM)	2			kV

Condition (1): 300 Ohms line termination resistor to GND.

Receiver

Parameter	Conditions	Min.	Typ.	Max.	Units
Absolute maximum voltage rating		0		5	V

AC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Pulse width		100			ns
Pulse rate		0		5	MHz
10%-90% rise/fall time	(1)		10	20	ns

Condition (1): Short cable (1 m) and a 300 Ohms line termination resistor to GND.

Logical Map

The state of the port is reported as follows:

Input voltage	Logical State
VIN > 2.0 V	HIGH
VIN < 0.8 V	LOW
Unconnected input port	*Undetermined*

Compatible sources

Sources with the following drivers are compatible:

- LVTTL (3.3 V low-voltage TTL)
- TTL (5 V TTL)
- CMOS (5 V CMOS)

Compatible loads

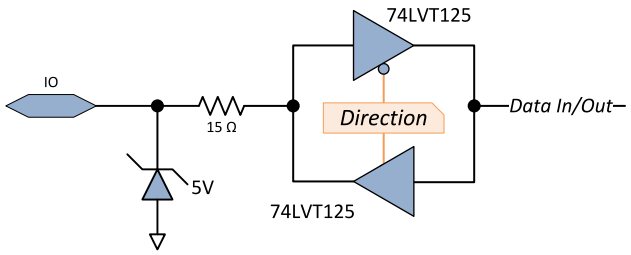
Loads with the following receivers are compatible:

- LVTTL (3.3 V low-voltage TTL)
- TTL (5 V TTL)

3.10. TTL Input/Output (Version 2)

Applies to:

Octo	QuadCXP12	MonoCXP12LH	DuoCXP12	3610	3612



TTL Input/Output Simplified schematic

The port implements a 3.3 V LVTTL driver and a 5 V-compliant 3.3 V LVTTL receiver.

DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
ESD protection	Human Body Model (HBM)	2			kV

NOTE
The I/O port includes a latch-up protection.

Driver

Parameter	Conditions	Min.	Typ.	Max.	Units
Low-level output current				64	mA
Low-level output voltage	@ 8 mA		0.34	0.36	V
	@ 16 mA		0.48	0.55	V
	@ 32 mA		0.78	0.81	V
	@ 64 mA		1.34	1.36	V
High-level output current				-32	mA
High-level output voltage	@-8 mA; (1)	2.60	3.00		V
	@-16 mA; (1)	2.20	2.70		V
	@-32 mA; (1)	1.75	2.20		V
ESD protection	Human Body Model (HBM)	2			kV

Condition (1): 300 Ohms line termination resistor to GND.

Receiver

Parameter	Conditions	Min.	Typ.	Max.	Units
Absolute maximum voltage rating		0		5	V

AC characteristics

Driver

Parameter	Conditions	Min.	Typ.	Max.	Units
Pulse width		100			ns
Pulse rate		0		5	MHz
10%-90% rise time			8		ns
10%-90% fall time			7.5		ns

Receiver

Parameter	Conditions	Min.	Typ.	Max.	Units
Pulse width		100			ns
Pulse rate		0		5	MHz

Logical Map

The state of the port is reported as follows:

Input voltage	Logical State
VIN > 2.0 V	HIGH
VIN < 0.8 V	LOW
Unconnected input port	*Undetermined*

Compatible sources

Sources with the following drivers are compatible:

- LVTTL (3.3 V low-voltage TTL)
- TTL (5 V TTL)
- CMOS (5 V CMOS)

Compatible loads

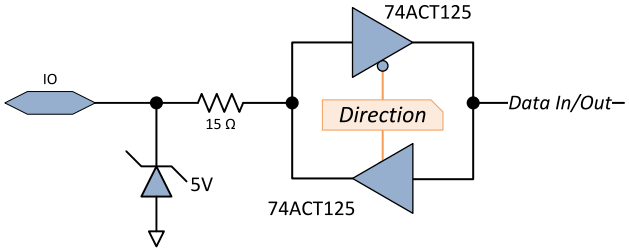
Loads with the following receivers are compatible:

- LVTTL (3.3 V low-voltage TTL)
- TTL (5 V TTL)

3.11. TTL Input/5 V CMOS Output

Applies to:

3612



TTL Input/5 V CMOS Output Simplified schematic

The port implements a 5 V CMOS driver and a TTL-compliant receiver.

DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
ESD protection	Human Body Model (HBM)	2			kV

NOTE
The I/O port includes a latch-up protection.

Driver

Parameter	Conditions	Min.	Typ.	Max.	Units
Absolute maximum voltage rating		0		5	V
Low-level output current				24	mA
Low-level output voltage	@50µA		0.001	0.1	V
	@ 24 mA			0.81	V
High-level output current				-24	mA
High-level output voltage	@-50 µA; (1)	4.9	4.99		V
	@-24 mA; (1)	3.89			V

Condition (1): 300 Ohms line termination resistor to GND.

Receiver

Parameter	Conditions	Min.	Typ.	Max.	Units
Absolute maximum voltage rating		0		5	V

AC characteristics

Driver

Parameter	Conditions	Min.	Typ.	Max.	Units
Pulse width		500			ns
Pulse rate		0		1	MHz
10%-90% rise/fall time			TBD		ns

Receiver

Parameter	Conditions	Min.	Typ.	Max.	Units
Pulse width		500			ns
Pulse rate		0		1	MHz
10%-90% rise/fall time			TBD		ns

Logical Map

The state of the port is reported as follows:

Input voltage	Logical State
VIN > 2.0 V	HIGH
VIN < 0.8 V	LOW
Unconnected input port	*Undetermined*

Compatible sources

Sources with the following drivers are compatible:

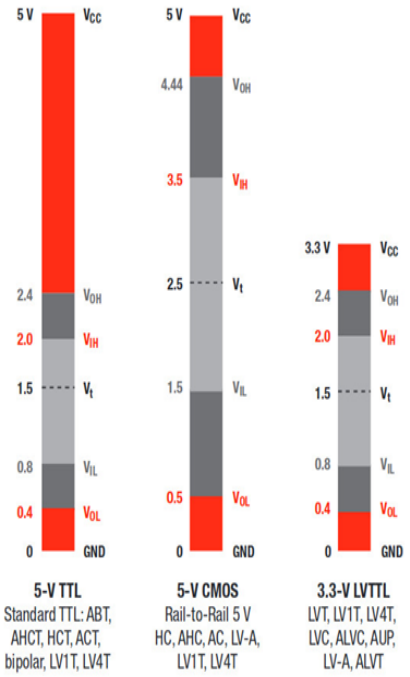
- LVTTL (3.3 V low-voltage TTL)
- CMOS (5 V CMOS)
- LVCMOS (3.3 V CMOS)

Compatible loads

Loads with the following receivers are compatible:

- TTL (5 V TTL)
- CMOS (5 V CMOS)

3.12. TTL, 5 V CMOS and LVTTL Levels



Colors legend

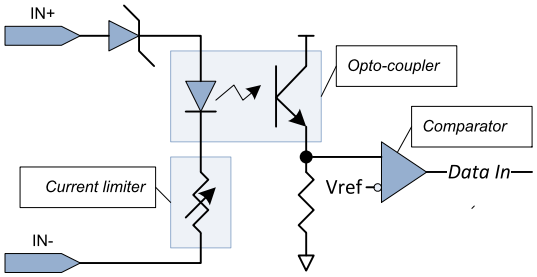
- Dark gray: noise margin,
- Light gray: transition range, low and high level are unspecified

Voltage levels

- $V_{IL:}$ maximum low-state voltage @receiver input
- VIH: minimum high-state voltage @receiver input
- $V_{OL:}$ maximum low-state voltage @driver output
- $V_{OH:}$ minimum high-state voltage @driver output
- V_t: threshold level, typically at the middle of the transition range

3.13. Isolated Input

Specification of the isolated GPIO input ports

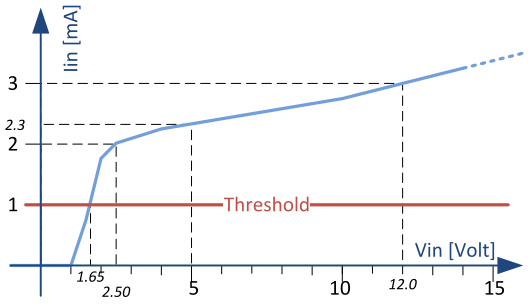


Isolated Input Simplified schematic

The input port implements an isolated current-sense input.

DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential voltage		-30		+30	V
Input current threshold			1		mA
Differential voltage	@1 mA	1.5	1.65	1.9	V
Input current	@(VIN+ - VIN-) = 1.65 V		1		mA
	@(VIN+ - VIN-) = 2.5 V		2		mA
	@(VIN+ - VIN-) = 5 V		2.3		mA
	@(VIN+ - VIN-) = 12 V		3		mA
	@(VIN+ - VIN-) = 30 V			5	mA
	@(VIN+ - VIN-) < 1 V			10	µA
DC isolation voltage		250			V
AC isolation voltage		170			V_{RMS}



Input Current vs. Input Voltage Characteristics

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	10			µs
Pulse rate	0		50	kHz

Logical map

The state of the port is reported as follows:

Input current	Logical State
IIN > 1 mA	HIGH
IIN < 1 mA	LOW
Unconnected input port	LOW

Compatible drivers and receivers

The following drivers are compatible with the isolated current-sense inputs:

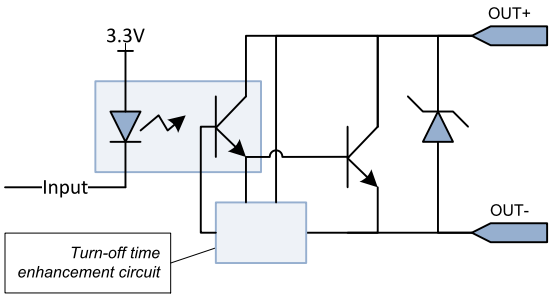
- Totem-pole LVTTL, TTL, 5 V CMOS drivers
- RS-422 Differential line drivers
- Potential free contact, solid-state relay, or opto-isolators
- 12 V and 24 V signaling voltages are also accepted

NOTE

- The +12 V power supply on the I/O connector(s) can be used for powering drivers requiring a power supply.
- No external resistors are required. However, to obtain the best noise immunity with 12 V and 24 V signaling, it is recommended to insert a series resistor in the circuit. The recommended resistor values are: 4.7k Ohms for 12 V signaling and 10k Ohms for 24 V signaling.

3.14. Isolated Output

Specification of the isolated GPIO output ports



Isolated Output Simplified schematic

The output port implements an isolated contact output.

DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Current				100	mA
Differential voltage	Open state	-30		30	V
	Closed state @ 1 mA			0.4	V
	Closed state @ 100 mA			1.0	V
DC isolation voltage		250			V
AC isolation voltage		170			V_{RMS}

NOTE

- The output port in the closed state has no current limiter, the user circuit must be designed to avoid excessive currents that could destroy the output port.
- The output port remains in the OFF-state until it is under control of the application.

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse rate	0		100	kHz
Turn-on time			5	µs
Turn-off time			5	µs

Typical switching performance @ 25°C

Current [mA]	Turn ON time [µs]	Turn OFF time [µs]
0.5	2.0	4.8
1.0	2.0	3.9
4.0	2.2	3.3
10	2.3	2.7
40	2.3	2.7
100	2.3	2.7

Logical map

The state of the output port is determined as follows:

Logical State	Output port state
HIGH	The contact switch is closed (ON)
LOW	The contact switch is open (OFF)

Compatible loads

The following loads are compatible with the isolated contact output ports:

- Any load within the 30 V / 100 mA envelope is accepted. The power originates from an external power source or alternatively from the power delivered through the 12 V and GND pins of the I/O connectors.

4. Environmental Specification

Environmental specification of the product(s) including: climatic requirements, electromagnetic standards compliance statements, safety standards compliance statements, etc.

4.1. Environmental Conditions

Storage and operating conditions specification of standard climatic class products

Storage Conditions

Applies to:

Mono | Duo | Quad | QuadG3 | QuadG3LH | QuadG3DF | Quad3DLLE | Octo | QuadCXP12 | QuadCXP12J | MonoCXP12LH | DuoCXP12 | 1625 | 1636 | 3303 | 3304 | 3610 | 3612 | 3614

Parameter	Conditions	Min	Max	Units
Ambient air temperature		-20 [-4]	70 [158]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

Operating Conditions

Applies to:

Mono | Duo | Quad | QuadG3 | QuadG3LH | QuadG3DF | Quad3DLLE | 1625 | 1636 | 3303 | 3304 | 3610 | 3612 | 3614

Parameter	Conditions	Min	Max	Units
FPGA die temperature			80 [176]	°C [°F]
Ambient air temperature		0 [32]	55 [131]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

Applies to:

Octo | QuadCXP12 | QuadCXP12J | MonoCXP12LH | DuoCXP12

Parameter	Conditions	Min	Max	Units
FPGA die temperature			95 [203]	°C [°F]
Ambient air temperature		0 [32]	55 [131]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

WARNING
The thermal design of the host PC must ensure that, at any time, the FPGA die temperature never exceeds the recommended limit.

WARNING
Exceeding the upper limit of the FPGA die temperature can permanently damage the card.

4.2. Temperature Monitor

FPGA die temperature sensor

All Coaxlink frame grabbers embed a temperature sensor on the FPGA die.

When the TemperatureSensorSelector feature of the Interface Module is set to Grabber, the Temperature feature of the Interface Module reports the FPGA die temperature expressed in °C.

The user application is invited to check regularly the FPGA die temperature to ensure that the board operates within the specified operating limits.

See also: "Environmental Conditions" on the previous page

FPGA die temperature warning

Applies to:
MonoCXP12LH DuoCXP12

When the measured FPGA die temperature reaches *87°C*, these Coaxlink products post a *"FPGA temperature is too high"* Memento message.

The *"FPGA temperature is too high"* message is sent repeatedly every second until the measured temperature decreases below 83°C or increases above 103°C.

TIP
Operation is still possible but is not recommended!

WARNING
When such event occurs, the user is invited to check and, possibly, improve the card cooling in the host PC!

FPGA die temperature error

Applies to:
MonoCXP12LH DuoCXP12

Random errors could occur in the FPGA if its core temperature becomes excessive. Therefore, for security reasons, the stream acquisition is stopped when the measured FPGA die temperature reaches 103°C!

The *"FPGA temperature is too high; stopping operation to prevent damaging the card"* Memento message is sent repeatedly every second until the measured temperature decreases below 97°C.

TIP
Stopping the acquisition reduces significantly the heat production of the FPGA. This action is aimed to reduce the die temperature, to prevent the application against unexpected FPGA behavior and to prevent damaging the card.

WARNING
When such event occurs, the user must immediately shut down the system and revise the card cooling in the host PC before restarting!

4.3. Thermal Data

The main heat contributors are:

1. The electronic devices of the Coaxlink card including the losses of the power converters of the *main* power distribution network.
2. The losses of the 12V-24 V power converter of the *auxiliary* power distribution network of Coaxlink PCIe products. The actual contribution depends on the effectively delivered PoCXP power!

> **NOTE**
> The losses of the 12V-24 V power converter are estimated with 17 W* of PoCXP output power per connector and a worst case 24 V DC/DC converter efficiency of 92.5%.
> (*) 25 W for **3621-LH Coaxlink Mono CXP-12 LH**

Generated heat power estimation and cooling method

The following table shows the estimated heat power generated by the card for two use cases:

1. *Heat power 1:* when the card doesn't deliver any PoCXP power
2. *Heat power 2:* when the card delivers the maximum PoCXP power on all connectors.

Product	Heat power 1	Heat power 2	Cooling method
1630 Coaxlink Mono	9.3 W	10.6 W	Air, heatsink with fan
1631 Coaxlink Duo	11.4 W	14.1 W	Air, heatsink with fan
1632 Coaxlink Quad	12.1 W	17.6 W	Air, heatsink with fan
1633 Coaxlink Quad G3	16.8 W	22.3 W	Air, heatsink with fan
1633-LH Coaxlink Quad G3 LH	16.8 W	22.3 W	Air, fanless heatsink
1635 Coaxlink Quad G3 DF	16.8 W	22.3 W	Air, heatsink with fan
1637 Coaxlink Quad 3D-LLE	16.8 W	22.3 W	Air, heatsink with fan
3602 Coaxlink Octo	16.0 W	27.0 W	Air, heatsink with fan
3603 Coaxlink Quad CXP-12	17.1 W	22.6 W	Air, heatsink with fan
3620 Coaxlink Quad CXP-12 JPEG	18.1 W	23.6 W	Air, heatsink with fan
3621-LH Coaxlink Mono CXP-12 LH	11.5 W	13.5 W	Air, fanless heatsink
3622 Coaxlink Duo CXP-12	14.8 W	17.5 W	Air, heatsink with fan

Requirements for air-cooled products with fan

The heat is dissipated into the ambient air inside the Host PC. The heat exchange is facilitated by a heat sink and a fan mounted on the FPGA (the component having the largest heat source).

The thermal design must ensure sufficient air flow along both sides to keep the FPGA die temperature below the upper limit of the allowed temperature range. The application is responsible for regularly checking the temperature and for taking the appropriate action in case of excessive temperature.

Requirements for fanless air-cooled products

The heat is dissipated into the ambient air inside the Host PC. The heat exchange is facilitated by a large heat sink mounted on the FPGA (the component having the largest heat source).

The thermal design must ensure sufficient the specified minimum air flow along both sides to keep the FPGA die temperature below the upper limit of the allowed temperature range. The application is responsible for regularly checking the temperature and for taking the appropriate action in case of excessive temperature.

4.4. Compliances

Compliance statements.

CE compliance statement

Applies to:

Mono	Duo	Quad	QuadG3	QuadG3LH	QuadG3DF
Quad3DLLE	Octo	QuadCXP12	QuadCXP12J	MonoCXP12LH	DuoCXP12
1625	1636	3303	3304	3610	3612
3614					

Notice for Europe

This product is in conformity with the Council Directive 2014/30/EU

This piece of equipment has been tested and found to comply with Class B EN55022/CISPR22 electromagnetic emission requirements and Class A EN55024/CISPR24 electromagnetic susceptibility.

This product has been tested in typical class A and class B compliant host systems. It is assumed that this product will also achieve compliance in any class A or class B compliant unit.

To meet EC requirements, shielded cables must be used to connect a peripheral to the card.

FCC compliance statement

Applies to:

Mono	Duo	Quad	QuadG3	QuadG3LH	QuadG3DF
Quad3DLLE	Octo	QuadCXP12	QuadCXP12J	MonoCXP12LH	DuoCXP12
1625	1636	3303	3304	3610	3612
3614					

Notice for USA

Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation or when the equipment is operated in a commercial environment.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

RoHS compliance statement

This product is in conformity with the European Union 2015/863 (ROHS3) directive, that stands for "the restriction of the use of certain hazardous substances in electrical and electronic equipment".

REACH statement

This product is in conformity with the European Union 1907/2006 (REACH) regulation.

WEEE statement

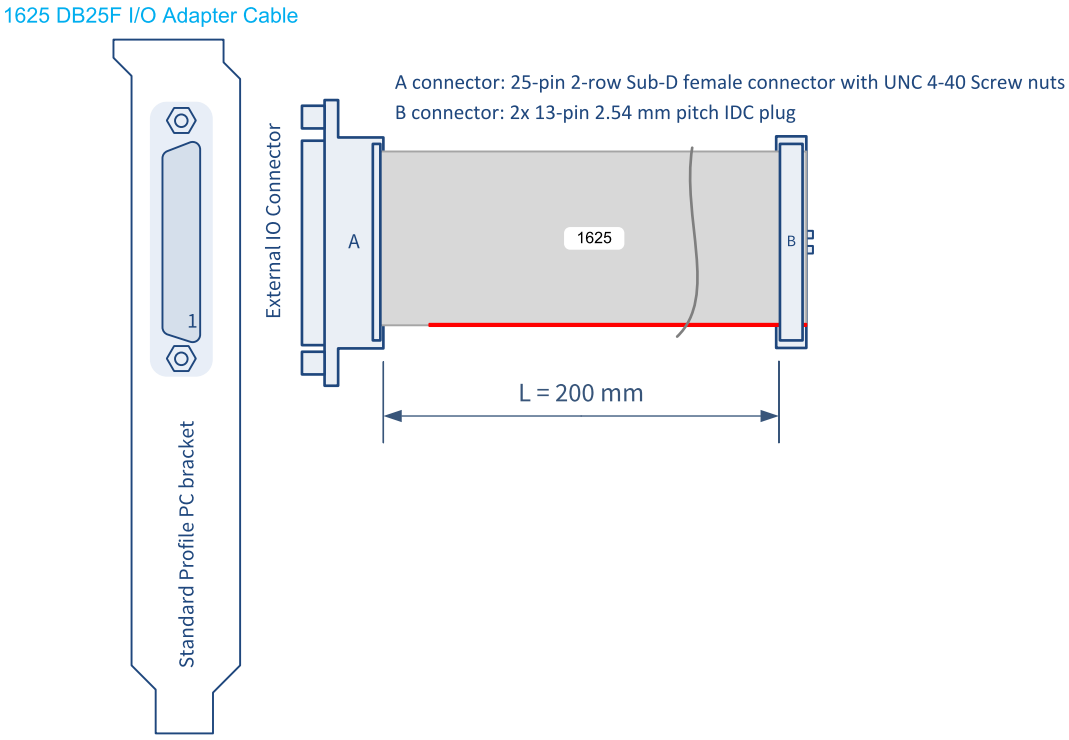
According the European Union 2012/19/EU directive, the product must be disposed of separately from normal household waste. It must be recycled according to the local regulations.

5. Related Products & Accessories

5.1. 1625 DB25F I/O Adapter Cable

Applies to:

Duo	Quad	QuadG3	QuadG3LH	QuadG3DF	Quad3DLLE
Octo	QuadCXP12	QuadCXP12J	MonoCXP12LH	DuoCXP12	



1625 DB25F I/O Adapter Cable

The **1625 DB25F I/O Adapter Cable** connects all the pins (but the pin 1) of a 26-pin dual-row 0.1" pitch connector to a 25-pin female SubD connector fitted into a standard-profile PC bracket.

Usage with Internal IO2 connector

The adapter brings the second set of I/O lines and the +12 V power output to a bracket-mount SubD connector. The pins are assigned as follows:

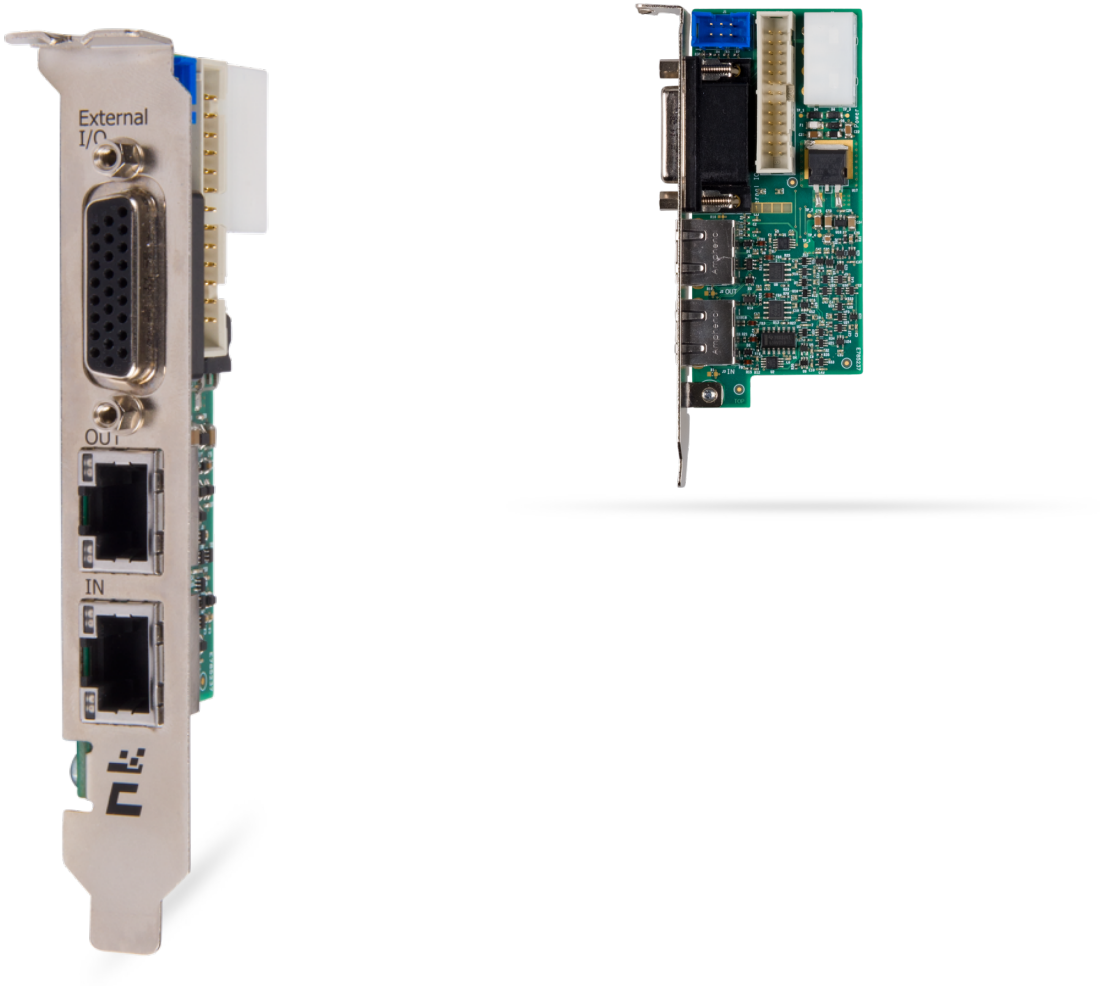
Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1		GND	Ground
2	2	1	GND	Ground
3	3	14	DIN21+	High-speed differential input #21 – Positive pole
4	4	2	DIN21-	High-speed differential input #21 – Negative pole
5	5	15	DIN22+	High-speed differential input #22 – Positive pole
6	6	3	DIN22-	High-speed differential input #22 – Negative pole
7	7	16	IIN21+	Isolated input #21 – Positive pole
8	8	4	IIN21-	Isolated input #21 – Negative pole
9	9	17	IIN22+	Isolated input #22 – Positive pole
10	10	5	IIN22-	Isolated input #22 – Negative pole
11	11	18	IIN23+	Isolated input #23 – Positive pole
12	12	6	IIN23-	Isolated input #23 – Negative pole
13	13	19	IIN24+	Isolated input #24 – Positive pole
14	14	7	IIN24-	Isolated input #24 – Negative pole
15	15	20	IOUT21+	Isolated contact output #21 – Positive pole
16	16	8	IOUT21-	Isolated contact output #21 – Negative pole
17	17	21	IOUT22+	Isolated contact output #22 – Positive pole
18	18	9	IOUT22-	Isolated contact output #22 – Negative pole
19	19	22	TTLIO21	TTL input/output #21
20	20	10	GND	Ground (TTLIO21 return)
21	21	23	TTLIO22	TTL input/output #22
22	22	11	GND	Ground (TTLIO22 return)
23	23	24	-	Not used
24	24	12	GND	Ground
25	25	25	+12V	+12 V Power output
26	26	13	GND	Ground (+12 V return)

Usage with Internal IO1 connector

The adapter brings the second set of I/O lines and the +12 V power output to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1		GND	Ground
2	2	1	GND	Ground
3	3	14	DIN11+	High-speed differential input #11 – Positive pole
4	4	2	DIN11-	High-speed differential input #11 – Negative pole
5	5	15	DIN12+	High-speed differential input #12 – Positive pole
6	6	3	DIN12-	High-speed differential input #12 – Negative pole
7	7	16	IIN11+	Isolated input #11 – Positive pole
8	8	4	IIN11-	Isolated input #11 – Negative pole
9	9	17	IIN12+	Isolated input #12 – Positive pole
10	10	5	IIN12-	Isolated input #12 – Negative pole
11	11	18	IIN13+	Isolated input #13 – Positive pole
12	12	6	IIN13-	Isolated input #13 – Negative pole
13	13	19	IIN14+	Isolated input #14 – Positive pole
14	14	7	IIN14-	Isolated input #14 – Negative pole
15	15	20	IOUT11+	Isolated contact output #11 – Positive pole
16	16	8	IOUT11-	Isolated contact output #11 – Negative pole
17	17	21	IOUT12+	Isolated contact output #12 – Positive pole
18	18	9	IOUT12-	Isolated contact output #12 – Negative pole
19	19	22	TTLIO11	TTL input/output #11
20	20	10	GND	Ground (TTLIO11 return)
21	21	23	TTLIO12	TTL input/output #12
22	22	11	GND	Ground (TTLIO12 return)
23	23	24	-	Not used
24	24	12	GND	Ground
25	25	25	+12V	+12 V Power output
26	26	13	GND	Ground (+12 V return)

5.2. 1636 InterPC C2C-Link Adapter



Pictures of 1636 InterPC C2C-Link Adapter

The **1636 InterPC C2C-Link Adapter** is an accessory product for use as an **InterPC C2C-Link extender** and/or as a **HD26F I/O adapter.**

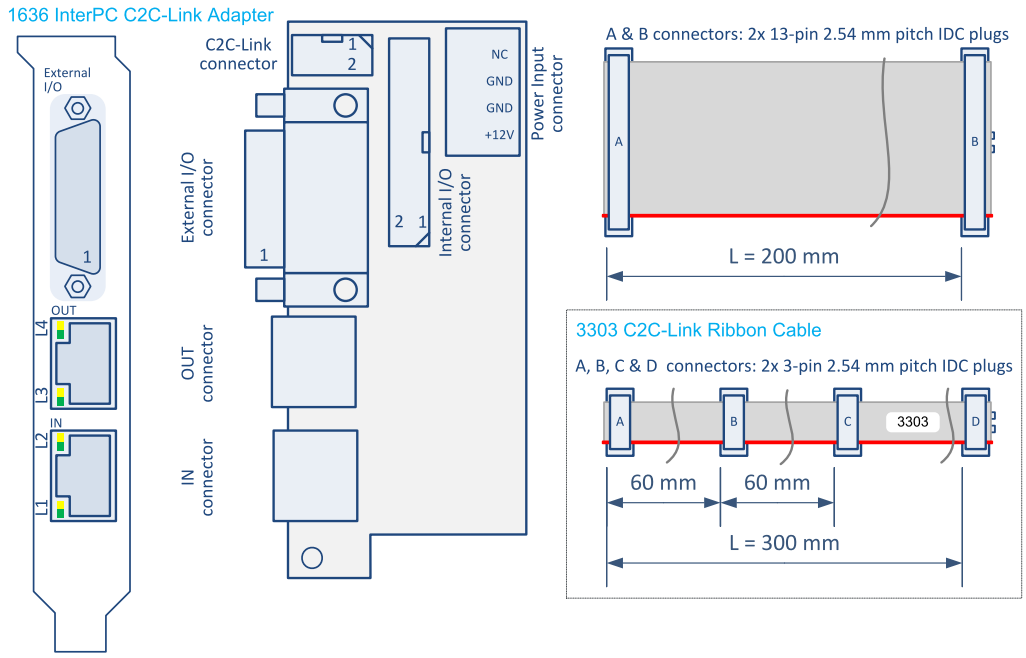
See also: "Hardware Description" on the next page for a hardware description of the C2C-Link extender.

See also: "Using 1636 as C2C-Link Extender" on page 116 for a description of the C2C-Link extender usage.

See also: "Using 1636 as HD26F I/O Adapter" on page 115 For a description of the HD26F I/O adapter usage

Hardware Description

Layout



1636 InterPC C2C-Link Adapter

The **1636 InterPC C2C-Link Adapter** product accessory is composed of:

- A printed circuit board assembly fitted with a standard-profile PC bracket.
- A 200-mm 26-way ribbon cable.
- A **3303 C2C-Link Ribbon Cable**.

Connectors

The **External I/O connector** is a HD26F – 26-pin 3-row high-density female – Sub-D connector fitted on the bracket with UNC 4-40 screws.

The **IN connector** and the **OUT connector** are RJ-45 8-pin sockets fitted on the bracket.

The **Internal I/O connector** is a 26-pin dual-row 0.1" pitch pin header with shrouding.

The **C2C-Link connector** is a 6-pin dual-row 0.1" pitch pin header with shrouding.

The **Internal I/O connector** is a 26-pin dual-row 0.1" pitch pin header with shrouding.

The **Power Input connector** is a 0.2" pitch right-angled Disk Drive Power connector.

See also: "Using 1636 as HD26F I/O Adapter" on the next page

See also: "Using 1636 as C2C-Link Extender" on page 116

See also: "Using 1636 as C2C-Link Extender" on page 116.

LEDs

The **IN connector** and the **OUT connector** are each equipped with 2 green/yellow LEDs named respectively **L1**, **L2**, **L3** and **L4**.

See also: "Using 1636 as C2C-Link Extender" on page 116.

Using 1636 as HD26F I/O Adapter

To use **1636 InterPC C2C-Link Adapter** as an HD26F I/O adapter:

- Plug the A-connector of the supplied 200-mm 26-way ribbon cable to the **Internal I/O** connector of the **1636 InterPC C2C-Link Adapter**
- Plug the B-connector to the **Internal I/O** connector of the target card.

NOTE
No power supply connection is required when using the **1636 InterPC C2C-Link Adapter** as an HD26F I/O adapter only.

Using 1636 as C2C-Link Extender

Adapter Powering

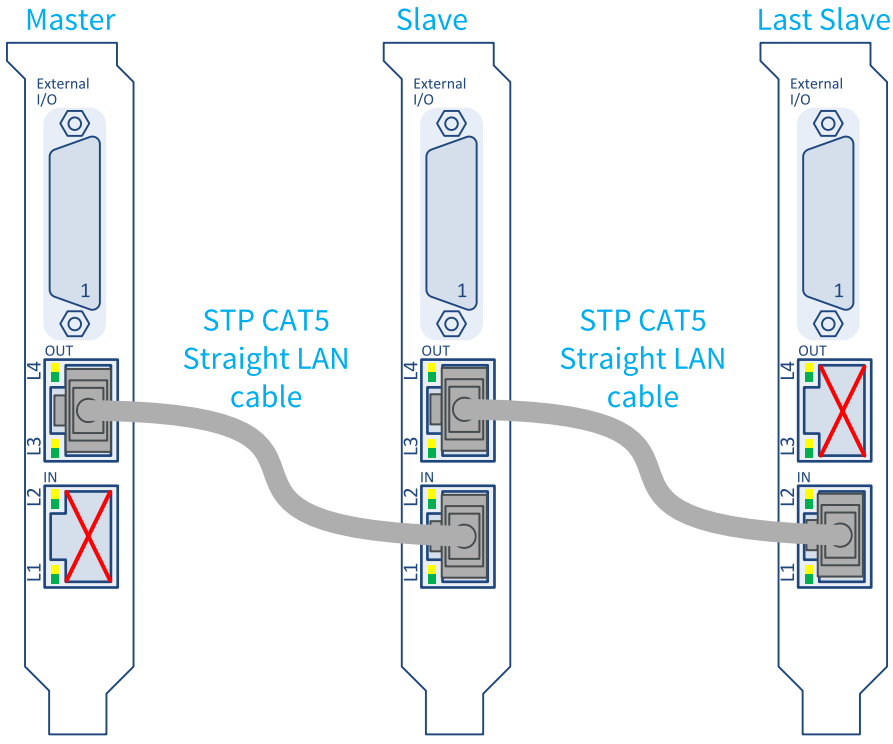
WARNING
The **1636 InterPC C2C-Link Adapter** must be powered when it is used as a C2C-Link extender.

The user has two options to supply power to the adapter:

- From the Coaxlink card +12 V power output through the 26-way ribbon cable attached to the **Internal I/O** connector.
- From the Host PC power supply through a Disk Drive Power connector cable plugged into the **Power Input connector**.

Parameter	Min.	Typ.	Max.	Units
+12 V DC Input voltage	11.0	12.0	13.0	V
+12 V Input power		1.8		W

InterPC Interconnect



External wiring of a C2C-Link across 3 adapters.

The external wiring of the C2C-Link is made with RJ 45 CAT 5 STP straight LAN cables. N-1 cables are required to interconnect N adapters in a daisy-chain scheme.

The daisy-chain begins on the OUT connector of the Master adapter and ends at the IN connector of the Last Slave adapter.

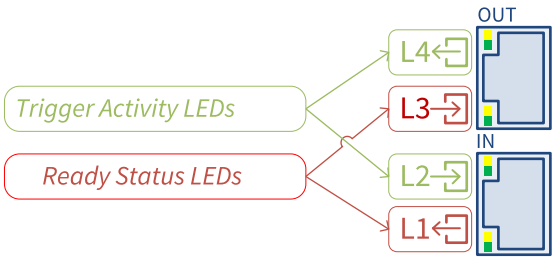
The IN connector of the Master adapter and the OUT connector of the Last Slave adapter are unused.

NOTE
The adapter disables the signal drivers of the IN and OUT connectors to avoid electrical damages when it detects a bad or a missing connection.

The InterPC cable drivers and receivers are not electrically isolated.

WARNING
To avoid damages, the interconnected PCs must have a common ground reference.

LEDs



1636 InterPC C2C-Link Adapter LEDs

Trigger Activity LEDs

The L2 and L4 LEDs indicate the trigger activity on the LAN cable. L2 shows the activity on the received trigger signals; L4 shows the activity on the transmitted trigger signals.

LED State	Indication
Off	The LAN cable is unplugged or the adapter is not powered.
Green	No trigger activity. *No trigger events in the past 10 milliseconds.*
Yellow	Trigger activity. *One or more trigger events in the past 10 milliseconds.*

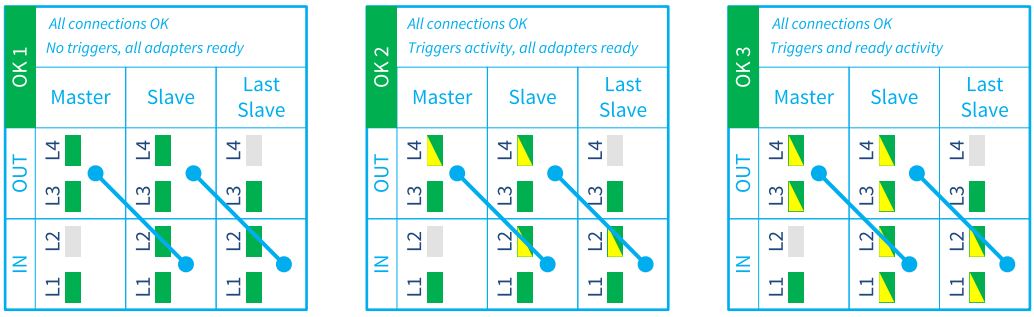
Ready Status LEDs

The L1 and L3 LEDs indicate the state of the ready signal on the LAN cable. L1 shows the state of the transmitted ready signal; L3 shows the state of the received ready signal.

LED State	Indication
Off	The adapter is not powered.
Green	Ready true. *For L1: all the C2C-Link devices attached to this adapter and the downwards adapters (if any) are ready.* *For L3: all the C2C-Link devices attached to the downwards adapters (if any) are ready.*
Yellow	Ready false. *For L1: one or more C2C-Link devices attached to this adapter and the downwards adapters (if any) are not ready.* *For L3: one or more C2C-Link devices attached to the downwards adapters (if any) are not ready.*

NOTE
Unlike the trigger activity LEDs, the ready signals are not enlarged. Short-duration not-ready states are hardly visible!

Adapters Array LED States – Normal Situations



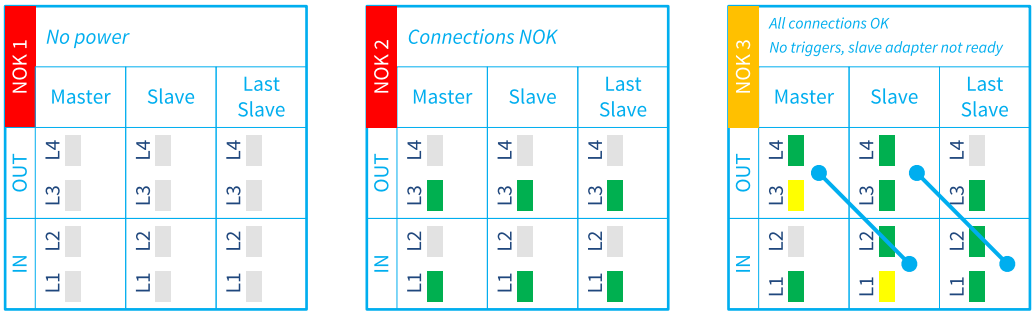
The above drawings show the LEDs states of 3 daisy-chained adapters for 3 normal situations.

In the OK 1 situation, all adapters are ready to accept triggers but no triggers are sent by the master.

In the OK 2 situation, the master adapter sends triggers and the ready signal of all adapters is permanently high. The yellow/green toggling L2 and L4 LEDs indicate the trigger activity. The steady green L1 and L3 LEDs indicate that all adapters are permanently ready to receive triggers.

In the OK 3 situation, the master adapter sends triggers and the ready signal of all adapters is cycling. The yellow/green toggling L2 and L4 LEDs indicate the trigger activity. The yellow/green toggling L1 and L3 LEDs indicate that all adapters are not ready to receive triggers for a significant duration.

Adapters Array LED States – Abnormal Situations



The above drawings show the LEDs states of 3 daisy-chained adapters for 3 abnormal situations.

In the NOK 1 situation, no adapters are powered. All LEDs are Off.

In the NOK 2 situation, all adapters are powered but all connections are missing or incorrect.

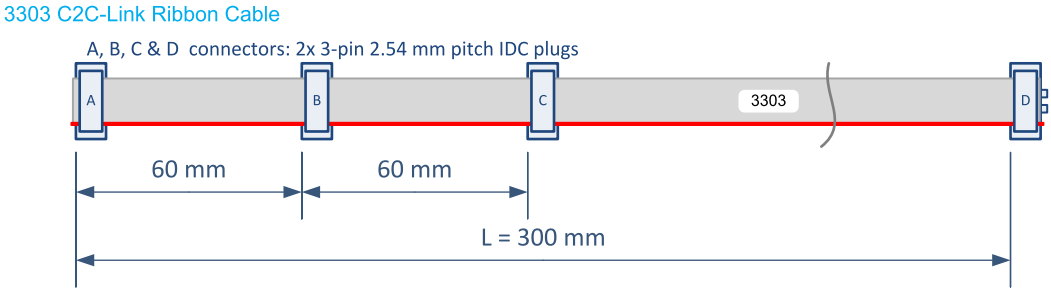
In the NOK 3 situation, all adapters are powered and all connections are OK, but the second adapter is not ready preventing the master to send new triggers. This situation is considered as abnormal when it persists.

Troubleshooting Guide

LEDs state	Indication and possible causes	Action
All LEDs Off	The adapter is not powered.	Apply power to the adapter
L2 Off L1 Green	The external connection to the IN connector is missing or incorrect.	For the master adapter, this is OK: nothing to do! For the other adapters: check and correct the connection to the OUT connector of the previous adapter in the daisy-chain.
L4 Off L3 Green	The external connection to the OUT connector is missing or incorrect.	For the last slave adapter of the daisy-chain, this is OK: nothing to do! For the other adapters: check and correct the connection to the IN connector of the next adapter in the daisy-chain.

5.3. 3303 C2C-Link Ribbon Cable

3303 C2C-Link Ribbon Cable is an accessory product used for Intra-PC C2C-Link interconnection.



3303 C2C-Link Ribbon Cable assembly

The **3303 C2C-Link Ribbon Cable** is a 6-conductor 0.05-in pitch ribbon fitted with 4 6-pin female ribbon cable connectors.

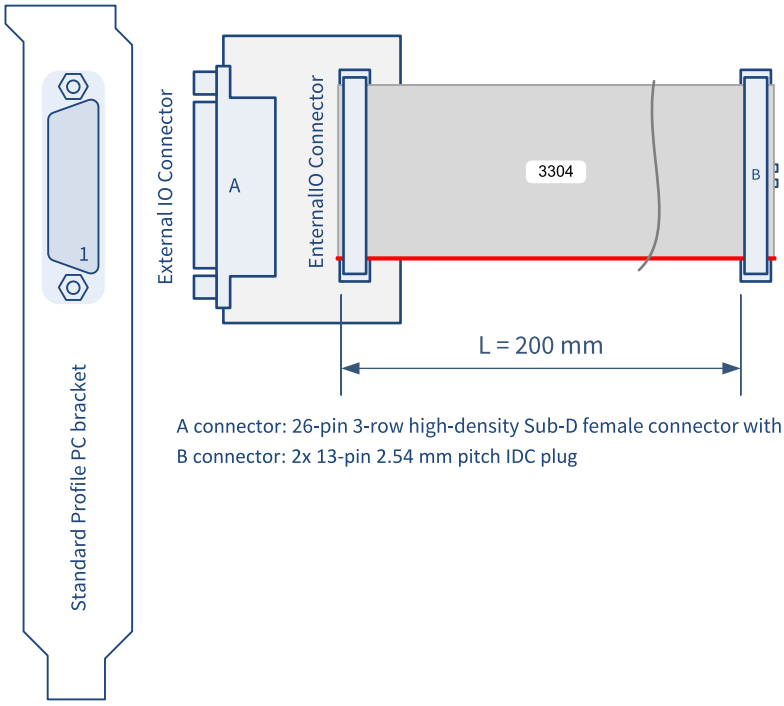
This cable is used for interconnecting the C2C-Link connectors of up to 4 cards located in the same PC.

5.4. 3304 HD26F I/O Adapter Cable

Applies to:

Duo	Quad	QuadG3	QuadG3LH	QuadG3DF	Quad3DLLE
Octo	QuadCXP12				

3304 HD26F I/O Adapter Cable



A connector: 26-pin 3-row high-density Sub-D female connector with UNC 4-40 Screw nuts
B connector: 2x 13-pin 2.54 mm pitch IDC plug

The **3304 HD26F I/O Adapter Cable** interconnects a 26-pin dual-row 0.1" pitch connector to a 26-pin 3-row female High-density SubD connector fitted into a standard-profile PC bracket.

Usage with Internal IO2 connector

Applies to:

Duo | Quad | QuadG3 | QuadG3LH | Quad3DLLE | QuadCXP12

The adapter brings the second set of I/O lines and the +12 V power output to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1	1	GND	Ground
2	2	10	GND	Ground
3	3	20	DIN21+	High-speed differential input #21 – Positive pole
4	4	19	DIN21-	High-speed differential input #21 – Negative pole
5	5	2	DIN22+	High-speed differential input #22 – Positive pole
6	6	11	DIN22-	High-speed differential input #22 – Negative pole
7	7	3	IIN21+	Isolated input #21 – Positive pole
8	8	12	IIN21-	Isolated input #21 – Negative pole
9	9	13	IIN22+	Isolated input #22 – Positive pole
10	10	21	IIN22-	Isolated input #22 – Negative pole
11	11	14	IIN23+	Isolated input #23 – Positive pole
12	12	4	IIN23-	Isolated input #23 – Negative pole
13	13	15	IIN24+	Isolated input #24 – Positive pole
14	14	5	IIN24-	Isolated input #24 – Negative pole
15	15	23	IOUT21+	Isolated contact output #21 – Positive pole
16	16	22	IOUT21-	Isolated contact output #21 – Negative pole
17	17	16	IOUT22+	Isolated contact output #22 – Positive pole
18	18	6	IOUT22-	Isolated contact output #22 – Negative pole
19	19	25	TTLIO21	TTL input/output #21
20	20	24	GND	Ground (TTLIO21 return)
21	21	17	TTLIO22	TTL input/output #22
22	22	7	GND	Ground (TTLIO22 return)
23	23	8	-	Reserved
24	24	9	GND	Ground
25	25	26	+12V	+12 V Power output
26	26	18	GND	Ground (+12 V return)

Usage with Internal IO1 connector

Applies to:

QuadG3DF | Octo

The adapter brings the second set of I/O lines and the +12 V power output to a bracket-mount SubD connector. The pins are assigned as follows:

Wire #	IDC Pin #	SubD Pin #	Signal Name	Signal Description
1	1	1	GND	Ground
2	2	10	GND	Ground
3	3	20	DIN11+	High-speed differential input #11 – Positive pole
4	4	19	DIN11-	High-speed differential input #11 – Negative pole
5	5	2	DIN12+	High-speed differential input #12 – Positive pole
6	6	11	DIN12-	High-speed differential input #12 – Negative pole
7	7	3	IIN11+	Isolated input #11 – Positive pole
8	8	12	IIN11-	Isolated input #11 – Negative pole
9	9	13	IIN12+	Isolated input #12 – Positive pole
10	10	21	IIN12-	Isolated input #12 – Negative pole
11	11	14	IIN13+	Isolated input #13 – Positive pole
12	12	4	IIN13-	Isolated input #13 – Negative pole
13	13	15	IIN14+	Isolated input #14 – Positive pole
14	14	5	IIN14-	Isolated input #14 – Negative pole
15	15	23	IOUT11+	Isolated contact output #11 – Positive pole
16	16	22	IOUT11-	Isolated contact output #11 – Negative pole
17	17	16	IOUT12+	Isolated contact output #12 – Positive pole
18	18	6	IOUT12-	Isolated contact output #12 – Negative pole
19	19	25	TTLIO11	TTL input/output #11
20	20	24	GND	Ground (TTLIO11 return)
21	21	17	TTLIO12	TTL input/output #12
22	22	7	GND	Ground (TTLIO12 return)
23	23	8	-	Reserved
24	24	9	GND	Ground
25	25	26	+12V	+12 V Power output
26	26	18	GND	Ground (+12 V return)

5.5. 3610/3612 I/O Extension Modules

Introduction

I/O extension modules extend the I/O capabilities of Coaxlink cards having the I/O extension feature. This topic describes two modules:

- **3610 HD26F I/O Extension Module TTL-RS422**
- **3612 HD26F I/O Extension Module TTL-CMOS5V-RS422**

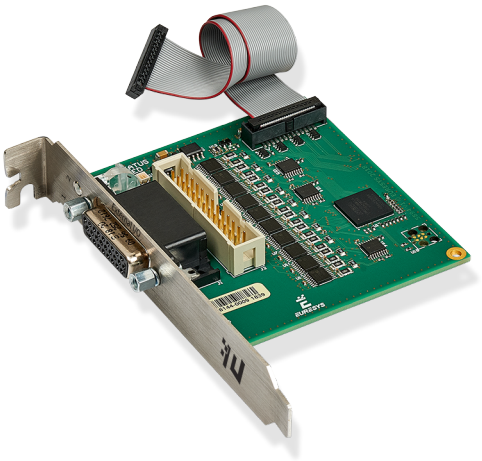
> **NOTE**
> The 3610 and the 3612 I/O extension modules are almost identical!
> They differ only by the electrical specification of the single-ended outputs:
> low-voltage 3.3 V TTL for 3610, 5 V CMOS for 3612.

These I/O extension modules are printed circuit board assemblies including:

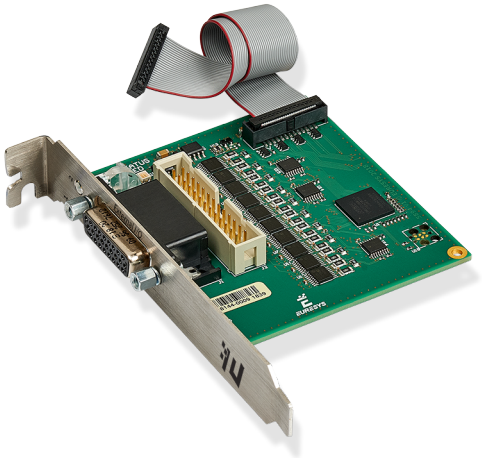
- a PC bracket fitted with SubD connector and LED indicators.
- a printed circuit board assembly implementing the I/O drivers and receivers and a control logic.
- a 26-pin high-density flat cable for direct connection to the I/O extension connector of the Coaxlink card.

Product pictures

They are powered by the Coaxlink card though the I/O extension cable.



3610 HD26F I/O Extension Module TTL-RS422



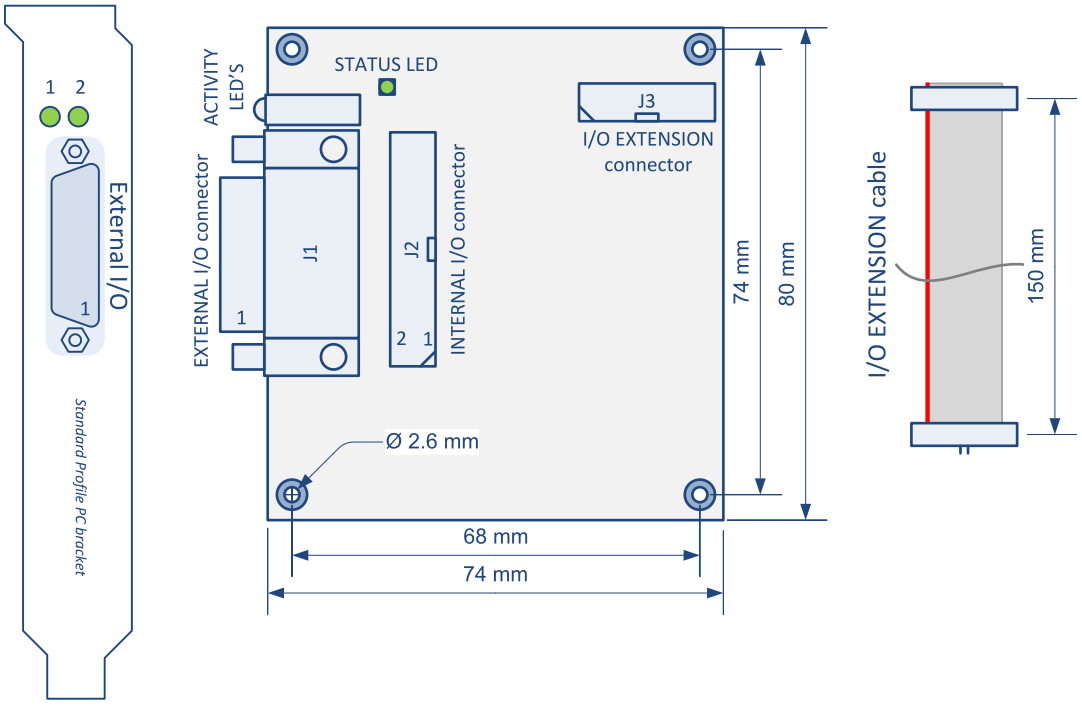
3612 HD26F I/O Extension Module TTL-CMOS5V-RS422

General specification

- configurable mix of 4 types of I/O ports:
  - single-ended 5 V compliant TTL input
  - single-ended 3.3 V LVTTL (3610 only) or 5 V CMOS (3612 only) output
  - differential RS-422 input
  - differential RS-422 output
- powered by the frame grabber through the I/O EXTENSION cable
- software configuration: no jumpers
- persistent configuration: the last configuration is automatically restored at power-up

WARNING
Hot plugging is not allowed!

Module layout



Connectors

- EXTERNAL I/O connector
  - Robust 26-pin high-density Sub-D
  - Compatible pin layout with *External I/O* connectors of Coaxlink cards for 12 V/GND and signals pairs

See also: "3610/3612 External I/O Connector" on page 34

- INTERNAL I/O connector
  - Standard pitch 26-pin flat cable header
  - Compatible pin layout with *Internal I/O* connectors of Coaxlink cards for 12 V/GND and signals pairs

See also: "3610/3612 Internal I/O Connector" on page 44

- I/O EXTENSION connector
  - Fine pitch 26-pin flat cable header fitted with the *I/O EXTENSION cable*: a 150 mm length flat cable for direct connection to the *I/O EXTENSION* connector of **3602 Coaxlink Octo** and **3603 Coaxlink Quad CXP-12** cards

See also: "I/O Extension Connector" on page 48

LEDs

Activity LED #1 on bracket

The ACTIVITY LED #1 is dedicated to the activity of input ports

LED State	Meaning
Green	Normal mode - Flashing indicates activity on at least one input.
Orange	Configuration mode
Red	Error - The I/O module is not (yet) controlled by the frame grabber
Off	The I/O module is not powered

Activity LED #2 on bracket

The ACTIVITY LED #2 is dedicated to the activity of output ports

LED State	Meaning
Green	Normal mode - Flashing indicates activity on at least one output.
Orange	Configuration mode
Red	Error - The I/O module is not (yet) controlled by the frame grabber
Off	The I/O module is not powered

Status LED on board

The STATUS LED is dedicated to the activity of the I/O extension bus

LED State	Meaning
Solid green	Normal mode - No activity on the bus.
Flashing green	Normal mode - Activity on the I/O extension bus.
Flashing orange	Configuration mode - Activity on the I/O extension bus.
Flashing red	Configuration mode - No activity on the I/O extension bus
Off	The I/O module is not powered

Electrical specifications

Specification Item	Product	
	3610	3612
Differential I/O	"Differential Input/Output" on page 83	
Single-ended I/O	"TTL Input/Output (Version 2)" on page 88	"TTL Input/5 V CMOS Output" on page 91
Power output	"I/O Power Output" on page 80	
Power consumption	< 5 W	

I/O configuration capabilities and constraints

Group	Single-ended I/O			Differential		
	I/O#	Input	Output	I/O#	Input	Output
Group #1	MIO1	2 x TTL in	2 x TTL out	MIO1	4 x RS-422 in	4 x RS-422 out
	MIO2					
	MIO3	2 x TTL in	2 x TTL out	MIO3		
	MIO4					
	MIO5	2 x TTL in	2 x TTL out	MIO5		
	MIO6					
	MIO7	2 x TTL in	2 x TTL out	MIO7		
	MIO8					
Group #2	MIO9	2 x TTL in	2 x TTL out	MIO9	4 x RS-422 in	4 x RS-422 out
	MIO10					
	MIO11	2 x TTL in	2 x TTL out	MIO11		
	MIO12					
	MIO13	2 x TTL in	2 x TTL out	MIO13		
	MIO14					
	MIO15	2 x TTL in	2 x TTL out	MIO15		
	MIO16					
Group #3	MIO17	2 x TTL in	2 x TTL out	MIO17	4 x RS-422 in	4 x RS-422 out
	MIO18					
	MIO19	2 x TTL in	2 x TTL out	MIO19		
	MIO20					

The 20 I/O ports are configurable by group. There are 3 groups:

- The group #1 contains **8 single-ended I/O ports** named MIO1 to MIO8 *OR* **4 differential I/O ports** MIO1, MIO3, MIO5, MIO7.
- The group #2 contains **8 single-ended I/O ports** named MIO9 to MIO16 *OR* **4 differential I/O ports** MIO9, MIO11, MIO13, MIO15.
- The group #3 contains **4 single-ended I/O ports** named MIO17 to MIO20 *OR* **2 differential I/O ports** MIO17 and MIO19.

Within a group, it is allowed to set *all* the I/O ports:

- for **differential input** operation *OR* ...
- for **differential output** operation*OR* ...
- for **single-ended** operation.

When the group is set for **single-ended** operation, it is allowed to set **each pair** of single-ended I/O:

- for input operation *OR* ...
- for output operation.

TIP
The configuration is saved into a non-volatile memory on the I/O module.
The configuration is automatically restored after applying power.

Software configuration

The IOExtensionModule category of the Interface module provides a set of features to configure the 3610/3612 I/O extension modules:

- IOExtensionModuleConfiguration to enter/leave configuration mode
- IOExtensionModuleLineSelector to select a MIO to configure
- IOExtensionModuleLineFormat, IOExtensionModuleLineMode and IOExtensionModuleLineStatus to configure the selected MIO
- IOExtensionModuleLineToRepair and IOExtensionModuleErrorCount to help troubleshoot an invalid current configuration.

Configuration procedure

1. Select an Interface module
2. Enter the configuration mode: set IOExtensionModuleConfiguration to Begin
3. Select the I/O line to configure: set IOExtensionModuleLineSelector to the desired value (MIO1 to MIO20)
4. Select the single-ended or differential I/O line format
   - For a single-ended I/O, set IOExtensionModuleLineFormat to TTL
   - For a differential I/O, set IOExtensionModuleLineFormat to DIFF
5. Select the input or output I/O line mode:
   - For an input, set IOExtensionModuleLineMode to Input
   - For an output, set IOExtensionModuleLineMode to Output
6. Repeat from steps 3 for all I/O's to configure
7. Verify the validity of the configuration
   - Get the value of IOExtensionModuleErrorCount
   - If 0, the configuration is OK, proceed to next step
   - If greater than 0, the configuration is NOK, proceed to step 10
8. Record the configuration
   - Set IOExtensionModuleConfiguration to Commit
   - The procedure is complete!
9. Repair the configuration
   - Get the value of IOExtensionModuleLineToRepair
   - Read "I/O configuration capabilities and constraints" on page 130 to determine why the indicated MIO doesn’t satisfy the configuration constraints.
   - Adapt the configuration of one (or more) I/O's accordingly by proceeding from step 3 .

Module information

The IOExtensionModuleInformation category of the Interface module provides information details.

- IOExtensionModuleSerialNumber
- IOExtensionModulePartNumber
- OExtensionModuleProductCode
- IOExtensionModuleRevision
- IOExtensionModuleVariant

5.6. 3614 I/O Extension Module

Applies to:

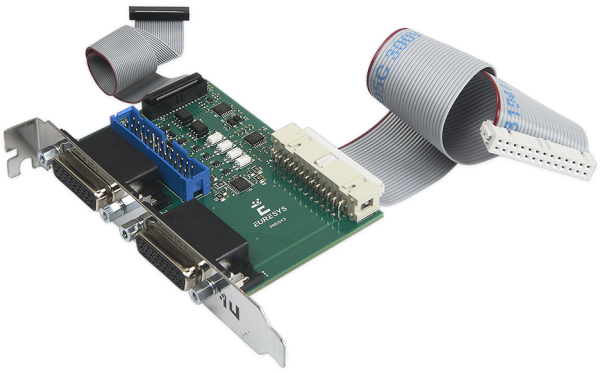
Octo | MonoCXP12LH | DuoCXP12

Introduction

This topic describes the **3614 HD26F I/O Extension Module - Standard I/O Set** accessory.

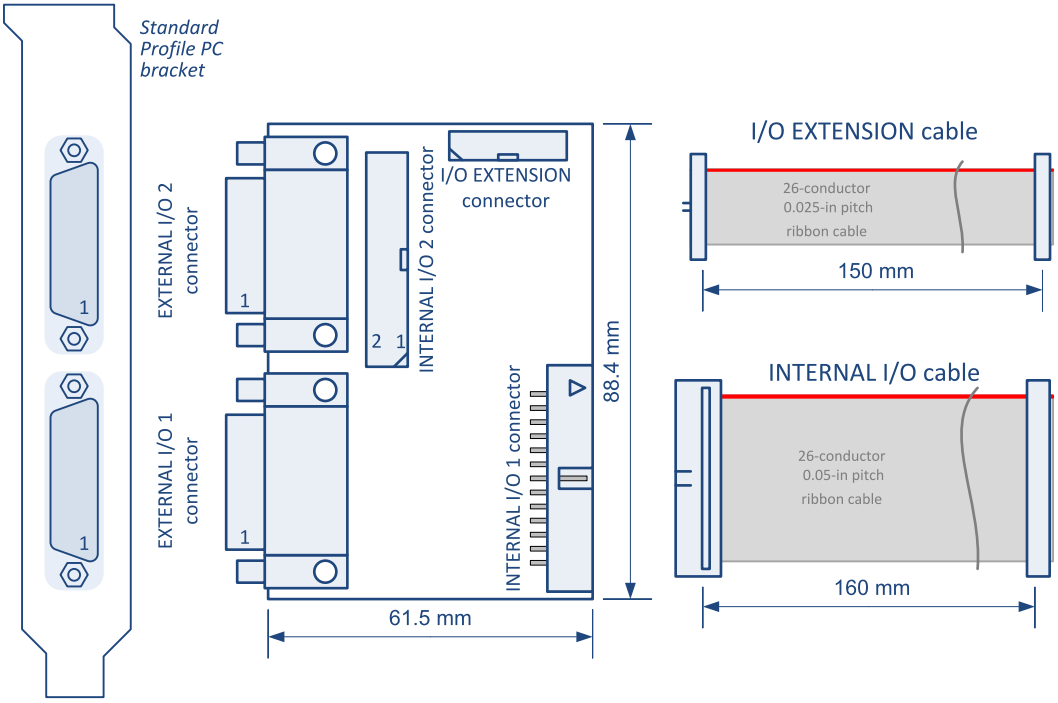
This I/O extension module adds a **second standard I/O set** of 10 I/O lines and provides an HD26F adapter for the **first standard I/O set.**

It allows users of above listed products to extend the number of I/O ports and to have all I/O ports on two robust HD26F Sub-D connector.



3614 I/O extension module assembly

Description



3614 I/O extension module layout

This I/O extension module includes:

- a PC bracket fitted with two 26-pin high-density female Sub-D connectors named EXTERNAL I/O 1 and EXTERNAL I/O 2,
- a printed circuit board assembly implementing five connectors and the I/O drivers and receivers of the second I/O set,
- a 26-pin high-density flat cable for direct connection to the I/O EXTENSION connector of the Coaxlink card,
- a 26-pin flat cable for direct connection to the INTERNAL I/O 1 connector of the Coaxlink card

This I/O extension module is powered by the Coaxlink card though the I/O extension cable.

Connectors

- EXTERNAL I/O 1 connector
  - Robust 26-pin high-density Sub-D
  - All I/O lines of the standard I/O set *#1*
  - Same pin layout as the *External I/O* connectors of Coaxlink cards

See also: "3614 External I/O 1 Connector" on page 36

- EXTERNAL I/O 2 connector
  - Robust 26-pin high-density Sub-D
  - All I/O lines of the standard I/O set *#2*
  - Similar pin layout as the *External I/O* connectors of Coaxlink cards

See also: "3614 External I/O 2 Connector" on page 38

- INTERNAL I/O 2 connector
  - Two-row 0.1 in pitch straight 26-pin flat cable header
  - All I/O lines of the standard I/O set *#2*
  - Same pin layout as the *Internal I/O* 2 connectors of Coaxlink cards

See also: "3614 Internal I/O 2 Connector" on page 46

- INTERNAL I/O 1 connector
  - Two-row 0.1 in pitch right-angled 26-pin flat cable header
  - For connection via the INTERNAL I/O cable to the "Internal I/O 1 Connector" on page 40 of **3602 Coaxlink Octo**
- I/O EXTENSION connector
  - Two-row 0.5 in pitch 26-pin straight flat cable header
  - For connection via the I/O EXTENSION cable to the to "I/O Extension Connector" on page 48of **3602 Coaxlink Octo**

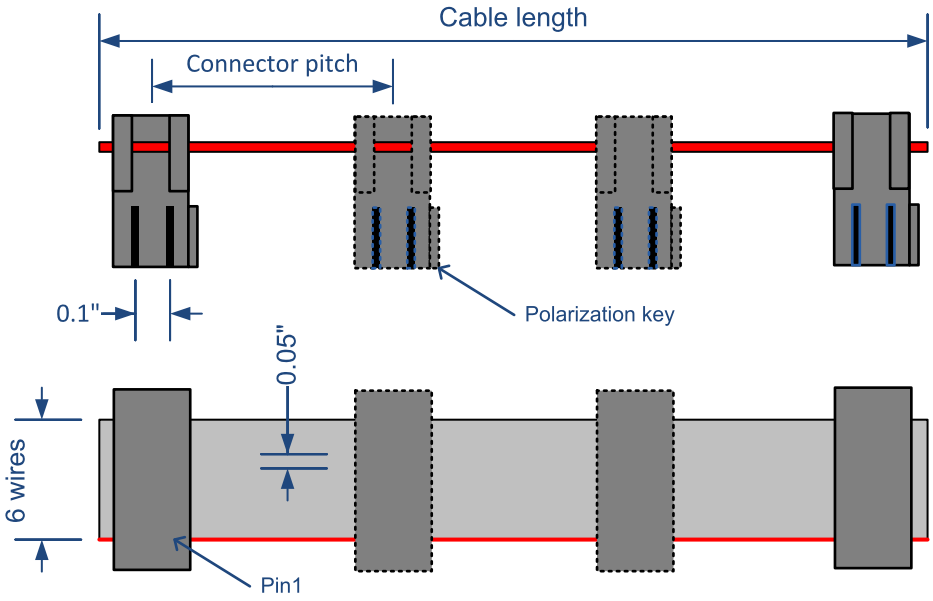
Electrical specifications

Item	Electrical Specification
Isolated inputs	"Isolated Input" on page 95
Isolated output	"Isolated Output" on page 98
Differential inputs	"Differential Input" on page 81
TTL I/O	"TTL Input/Output (Version 1)" on page 85
I/O Power output	"I/O Power Output" on page 80

NOTE
The electrical specifications are identical for I/O set #1 and I/O set #2!

5.7. Custom C2C-Link Ribbon Cable Assembly

Assembly instructions of a custom-made IntraPC C2C-Link interconnection.



Custom C2C-Link Ribbon Cable Assembly

The cable assembly is composed with:

- A piece of a 6-conductor 0.05-in pitch ribbon cable. For instance: *Belden's (9L280XX Series)*.
- Two or more pieces of a 2 x 3-pin female ribbon cable connectors. For instance: *TE connectivity 1-1658528-1*.

The cable assembly has:

- A maximum of 4 connectors allowing up to 4 cards to share the same C2C-Link.
- A maximum length of 60 cm.

NOTE
The connector pitch(es) must be determined according to the actual card to card spacing in the Host PC.