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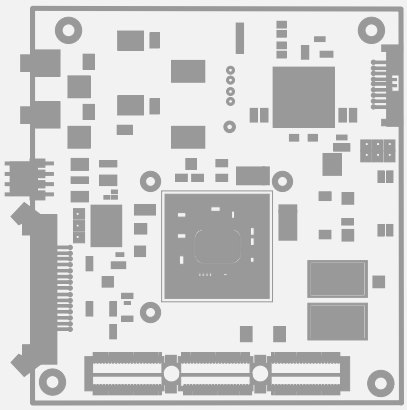
HARDWARE MANUAL

Coaxlink

Coaxlink Hardware Manual (PCIe/104 bus type)

1629 Coaxlink Duo PCIe/104-EMB
1634 Coaxlink Duo PCIe/104-MIL
3300 HD26F I/O module for Coaxlink Duo PCIe/104
3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104
3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104



Terms of Use

This documentation is provided with Coaxlink 12.5.4 (doc build 2109).
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Contents

1. About This Document

1.1. Document Scope

NOTE
This document describes the *hardware specifications* of the following products of the Coaxlink series together with their related products.

Coaxlink main products

Product	S/N Prefix	Icon
1629 Coaxlink Duo PCIe/104-EMB	KDI	Duo104EMB
1634 Coaxlink Duo PCIe/104-MIL	KDR	Duo104MIL

Related accessory products

Product	S/N Prefix	Icon
3300 HD26F I/O module for Coaxlink Duo PCIe/104	KDM	3300
3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104		3301
3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104		3302

NOTE
The S/N prefix is a 3-letter string at the beginning of the card serial number.

NOTE
Icons are used in this document for tagging titles of card-specific content.

1.2. Document Changes

Coaxlink 12.5

Interactive pin assignments table for all connectors (HTML only)

The following topic were revised:

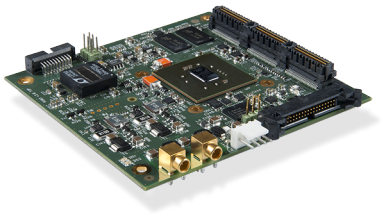
- "PCI Express Power" on page 37
- "Thermal Data" on page 55

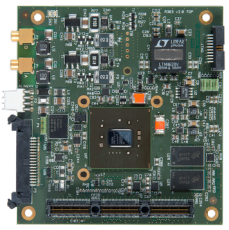
2. Mechanical Specification

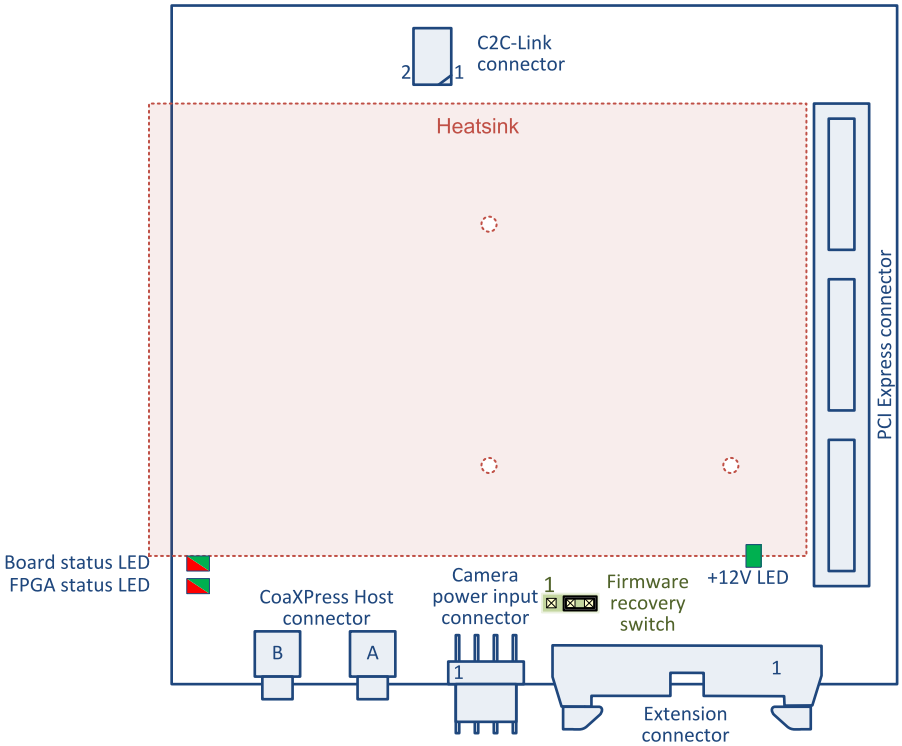
Mechanical specifications of the product(s) including: product pictures, physical dimensions, connectors description and pin assignments, LEDs description, switches description, etc.

2.1. Board and Bracket Layouts

1629 Coaxlink Duo PCIe/104-EMB and 1634 Coaxlink Duo PCIe/104-MIL







- "CoaXPress Host A Connector" on page 12
- "CoaXPress Host B Connector" on page 13
- "C2C-Link Connector" on page 16
- "12 V LED " on page 21
- "Board Status LED" on page 22
- "FPGA Status LED" on page 23
- "Firmware Recovery Switch" on page 24

2.2. Connectors

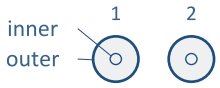
3302 DIN 2 CoaXPress Host Connector

Applies to:

3302

Connector description

Property	Value
Name	CoaXPress Host
Type	2 x DIN 1.0/2.3 75 Ohms coaxial receptacles
Location	Module-to-chassis coaxial cables
Usage	CoaXPress Host Interface



Pin assignments

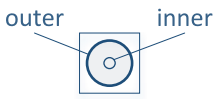
Pin	Signal	Usage
Inner1	CXP_A	CoaXPress Host Connection A
Outer1	GND	Ground
Inner2	CXP_B	CoaXPress Host Connection B
Outer2	GND	Ground

CoaXPress Host A Connector

Applies to:
Duo104EMB Duo104MIL

Connector description

Property	Value
Name	CoaXPress Host A
Type	MCX 75 Ohms coaxial female receptacle
Location	Printed circuit board
Usage	CoaXPress Host Interface



Pin assignments

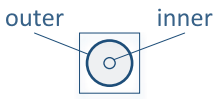
Pin	Signal	Usage
Inner	CXP_A	CoaXPress Host Connection A
Outer	GND	Ground

CoaXPress Host B Connector

Applies to:
Duo104EMB Duo104MIL

Connector description

Property	Value
Name	CoaXPress Host B
Type	MCX 75 Ohms coaxial female receptacle
Location	Printed circuit board
Usage	CoaXPress Host Interface



Pin assignments

Pin	Signal	Usage
Inner	CXP_B	CoaXPress Host Connection B
Outer	GND	Ground

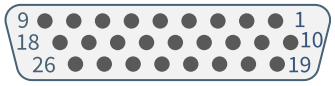
3300 I/O Connector

Applies to:

3300

Connector description

Property	Value
Name	I/O
Type	26-pin 3-row high-density female sub-D connector
Location	Remote I/O module
Usage	General purpose I/O and power output



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	DIN12+	High-speed differential input #12 – Positive pole
3	IIN11+	Isolated input #11 – Positive pole
4	IIN13-	Isolated input #13 – Negative pole
5	IIN14-	Isolated input #14 – Negative pole
6	IOUT12-	Isolated contact output #12 – Negative pole
7	GND	Ground
8		Not connected
9	GND	Ground
10	GND	Ground
11	DIN12-	High-speed differential input #12 – Negative pole
12	IIN11-	Isolated input #11 – Negative pole
13	IIN12+	Isolated input #12 – Positive pole
14	IIN13+	Isolated input #13 – Positive pole
15	IIN14+	Isolated input #14 – Positive pole

Pin	Signal	Usage
16	IOUT12+	Isolated contact output #12 – Positive pole
17	TTLIO12	TTL input/output #12
18	GND	Ground
19	DIN11-	High-speed differential input #11 – Negative pole
20	DIN11+	High-speed differential input #11 – Positive pole
21	IIN12-	Isolated input #12 – Negative pole
22	IOUT11-	Isolated contact output #11 – Negative pole
23	IOUT11+	Isolated contact output #11 – Positive pole
24	GND	Ground
25	TTLIO11	TTL input/output #11
26	+12V	+12 V Power output

C2C-Link Connector

Applies to:
Duo104EMB Duo104MIL

Connector description

Property	Value
Name	C2C-Link
Type	6-pin dual-row 0.1" pitch pin header with shrouding
Location	Printed circuit board
Usage	Card-to-card link

Pin assignments

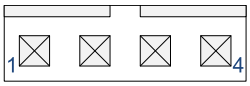
Pin	Signal	Usage
1	GND	Ground
2	CSync1	Card-to-card synchronization bus – Signal 1
3	GND	Ground
4	CSync2	Card-to-card synchronization bus – Signal 2
5	GND	Ground
6	CSync3	Card-to-card synchronization bus – Signal 3

Camera Power Input Connector

Applies to:
Duo104EMB Duo104MIL

Connector description

Property	Value
Name	Camera Power Input
Type	4-pin 0.1-in Molex KK 7478 male connector
Location	Printed circuit board
Usage	DC power input for PoCXP



Pin assignments

Pin	Signal	Usage
1	GND	Ground
2	+24V0	+24 VDC input
3	+24V0	+24 VDC input
4	GND	Ground

2.3. LEDs

CoaXPress LED lamps

Each connector of the CoaXPress Host Interface is associated with a LED lamp mounted on the bracket (for PCie cards only).

LED lamps mode control

The LampMode feature of the Interface module defines the lamps operation mode:

- When set to Standard (default value), the lamps indicate the state of the CoaXPress Link connection.
- When set to Dark, all lamps are turned off.
- When set to Error, all lamps are turned off unless error conditions are detected.
- When set to Custom, all lamps are controlled by LampCustomValue, a bitfield where each bit is mapped onto a lamp with 1 for orange and 0 for off by the LampCustomLedA … LampCustomLedH boolean features.

CoaXPress Host Indicator LED lamps states

States description

Symbol	Indication	State
	Off	No power
	Solid orange	System booting
	AlternateFlash_12_5 green / orange[1]	Connection detection in progress; PoCXP active
	Flash_12_5 orange[2]	Connection detection in progress; PoCXP not in use
	AlternateFlash_0_5 red / green	Device/ Host incompatible; PoCXP active
	AlternateFlash_0_5 red / orange	Device/ Host incompatible; PoCXP not in use

[1]Shown for a minimum of 1 second even if the connection detection is faster

[2]Shown for a minimum of 1 second even if the connection detection is faster

Symbol	Indication	State
	Solid red	PoCXP over-current
	Solid green	Device / Host connected, but no data being transferred
	Flash_1 orange	Device / Host connected, waiting for event (e.g. trigger, exposure pulse)
	Flash_12_5 green	Device / Host connected, data being transferred
	500 ms red pulse[1]	Error during data transfer (e.g. CRC error, single bit error detected)
	AlternateFlash_0_5 green / orange	Connection test packets being sent
	Flash_12_5 red	System error (e.g. internal error)

Flashing states timing definitions

Indication	Frequency	Duty Cycle
Flash_12_5	12.5 Hz	25% (20 milliseconds on, 60 milliseconds off)
Flash_1	1 Hz	20% (200 milliseconds on, 800 milliseconds off)
Flash_0_5	0.5 Hz	50% (1 second on, 1 second off)
AlternateFlash_12_5	12.5 Hz	25% (20 milliseconds on color 1, 60 milliseconds off, 20 milliseconds on color 2, 60 milliseconds off)
AlternateFlash_0_5	0.5 Hz	50% (1 second on color 1, 1 second off, 1 second on color 2, 1 second off)

[1]In case of multiple errors, there shall be at least two green Flash_12_5 pulses before the next error is indicated

12 V LED Duo104EMB Duo104MIL

12 V LED states

LED state	Symbol	Meaning
Off		**No 12 V power.** Possible causes are: • There is no power delivered on the +12 V rail of the PCIe/104 connector • The +12 V fuse is blown on the card
Solid green		**12 V power OK.**

Board Status LED

Board status LED indicator states

LED state	Symbol	Meaning
Off		**No power.** The board is not powered or the power distribution network is not functional.
Solid green		**Board status OK.** The main power distribution network is operational and the FPGA start-up procedure has successfully completed.
Solid red		**Board status NOK.** Possible causes are: • There is no power delivered on the +12 V rail of the PCI Express connector slot • The FPGA start-up procedure is not completed. *The normal completion time is around 100 milliseconds.* • At least one power converter of the main power distribution network is unable to operate properly. *This might be caused by excessive temperature due to inadequate board cooling, accidental short-circuits having blown one (or more) protection fuses, inappropriate supply voltages, etc.*

FPGA Status LED

FPGA status LED indicator states

LED state	Symbol	Meaning
Off		**Board not powered.**
Solid green		**FPGA status OK.** All the FPGA clock networks and the DDR memory are operating normally.
Solid red		**FPGA status NOK.** Possible causes are: • At least one FPGA clock network is not operating normally. *This might be caused by excessive jitter on external clock signals of the CoaXPress or the PCI Express interfaces.* • The DDR memory controller has not been able to successfully perform the calibration procedure.

2.4. Firmware Recovery Switch

Introduction

The firmware recovery switch is implemented with a 3-pin 1-row header and a jumper. The jumper has two positions: *normal* and *recovery*.

Normal position

At the next power ON, the latest firmware successfully written into the Flash EEPROM is used to program the FPGA.

After FPGA startup completion, the card exhibits the standard PCI ID and the Coaxlink driver allows normal operation.

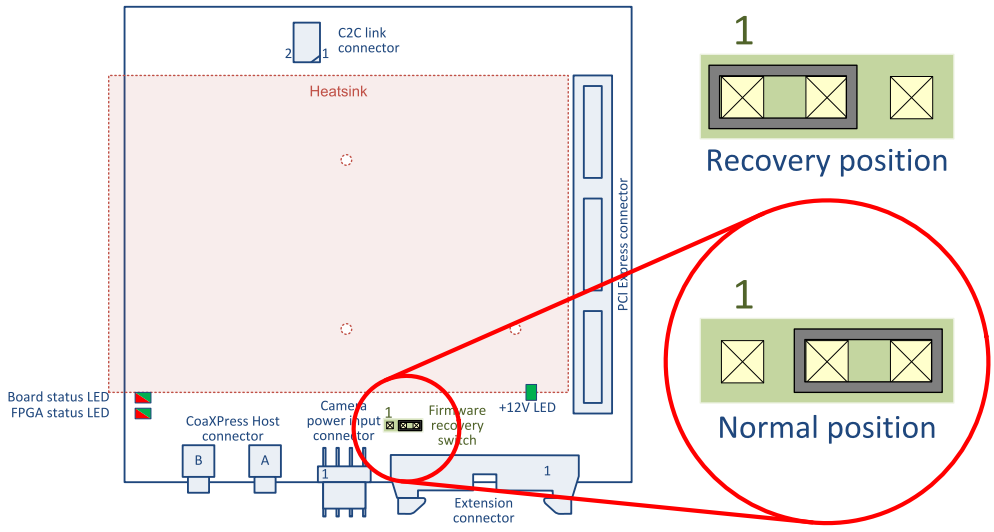
This is the factory default jumper position.

Recovery position

At the next power ON, the last but one firmware successfully written into the Flash EEPROM is used to program the FPGA.

After FPGA startup completion, the card exhibits the recovery PCI ID and the Coaxlink driver inhibits image acquisition.

1629 Coaxlink Duo PCIe/104-EMB, 1634 Coaxlink Duo PCIe/104-MIL



2.5. Physical Characteristics

Dimensions and weight

Product	Length	Width	Weight
1629 Coaxlink Duo PCIe/104-EMB	96 mm, 3.775 in	90 mm, 3.555 in	75 g, 2.65 oz
1634 Coaxlink Duo PCIe/104-MIL	96 mm, 3.775 in	90 mm, 3.555 in	75 g, 2.65 oz
3300 HD26F I/O module for Coaxlink Duo PCIe/104	70 mm, 2.76 in	40 mm, 1.57 in	60 g, 2.12 oz
3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104	86.8 mm, 3.42 in	60 mm, 2.36 in	75 g, 2.65 oz

Cable length

Product Item	Length
3300 HD26F I/O module for Coaxlink Duo PCIe/104 – Cable	254 mm, 10 in
3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104	200 mm, 7.9 in

3D CAD models

3D CAD models are available on request for the following assemblies:

Assembly	File formats
1629 Coaxlink Duo PCIe/104-EMB	DWF, STP
1629 Coaxlink Duo PCIe/104-EMB with **3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104**	DWF, STP
3300 HD26F I/O module for Coaxlink Duo PCIe/104	DWF, STP

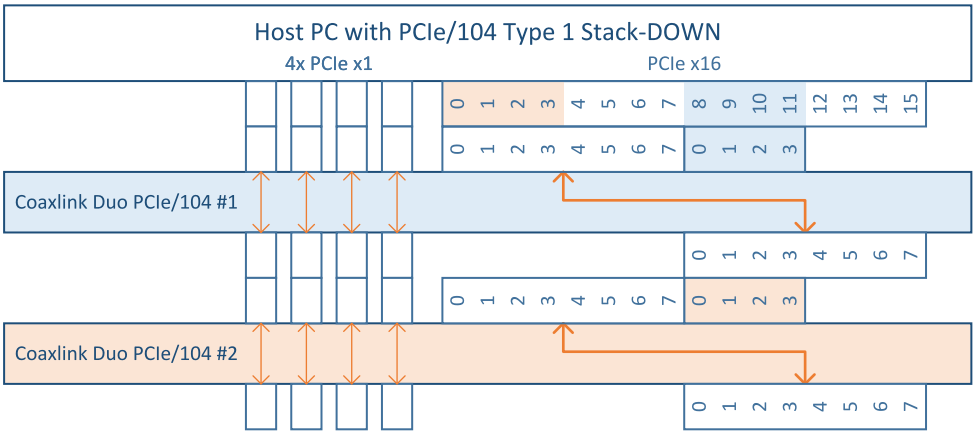
2.6. PCIe/104 Stacking Rules

One or two **1629 Coaxlink Duo PCIe/104-EMB** or **1634 Coaxlink Duo PCIe/104-MIL** modules can be stacked directly under the Host PC.

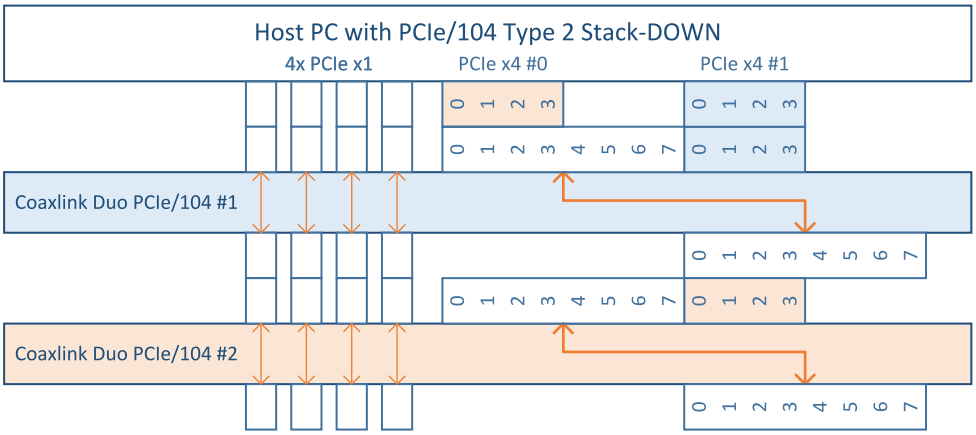
The Host PC must be equipped with one *stack-down* connector of the following types:

- Type 2 PCIe/104 with 2 PCI Express x4 links providing four active lanes.
- Type 1 PCIe/104 with 1 PCI Express x16 link configured to operate as 2 x8 links providing at least four active lanes per link.

NOTE
According the PCIe/104 specification, a Type 1 PCIe/104 host PC that supports a PCIe x16 link is not required to support two x8, or two x4 links. For such PCs, only one module can be stacked underneath!



PCIe/104 stack with a Type 1 Host PC and 2 modules.



PCIe/104 stack with a Type 2 Host PC and 2 modules.

Each module:

- Uses only 4 PCI Express lanes.
- Routes to the next module the 4 unused PCI Express x1 links.
- Shifts by 8 positions and routes to the next module the lowest 8 lanes of the PCI Express x16 link.
- Re-drives the clock of the Type 1 PCI Express x16 or the Type 2 PCI Express x4 links.

3. Electrical Specification

Electrical specification of the product(s) including: electrical characteristics of all the input/output ports, description of the power distribution, power requirements, etc.

3.1. CoaXPress Host Interface

Electrical specification of the CoaXPress Host interface

CoaXPress Host Interface Type per Product

Each connection of the CoaXPress Host interface implements a *Host Transceiver* (HT) and a *Power Transmitting Unit* (PTU).

Product	HT Type
1629 Coaxlink Duo PCIe/104-EMB	"CXP-6 Host Transceiver" below
1634 Coaxlink Duo PCIe/104-MIL	"CXP-6 Host Transceiver" below

CXP-6 Host Transceiver

Applies to:
Duo104EMB Duo104MIL

The Host transceiver implements a *high-speed cable receiver* and a *low-speed cable driver* for *CXP-6* speeds.

It fulfills the electrical specification of the CoaXPress 1.1 standard. Namely:

- The cable receiver requirements for the high-speed connection described in Table 2 of the Annex B of the CoaXPress Standard 1.1
- The cable driver requirements for the low-speed connection described in Table 3 of the Annex B of the CoaXPress Standard 1.1

Host Transceiver Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
High-speed connection bit rate		1.25		6.25	GT/s
Low-speed connection bit rate			20.833		MT/s
Max. cable length	BELDEN 1694 @ 1.25 GT/s	130			m
	BELDEN 1694 @ 2.5 GT/s	110			m
	BELDEN 1694 @ 3.125 GT/s	100			m
	BELDEN 1694 @ 5 GT/s	60			m
	BELDEN 1694 @ 6.25 GT/s	40			m

Power Transmitting Unit

The Power Transmitting Unit provides 17 W* of 24 V DC power per connection, over-current protection (OCP) and PoCXP device detection as specified by the CoaXPress Standard.

Power Transmitting Unit Specification

Parameter	Min.	Typ.	Max.	Unit
DC output voltage	22	24	26	V
Available output power	17*			W
OCP holding current	790			mA
OCP nominal trip current			5	A
Device detection sense resistance		4.7		kΩ

NOTE
(*) 25 W for **3621-LH Coaxlink Mono CXP-12 LH**

NOTE
The above specification applies over the whole operating temperature range of the Coaxlink card.

See also: Refer to Power Over CoaXPress in the Functional Guide

3.2. PCI Express Interface

Specification of the PCI Express Interface

The PCI Express Interface implements a *PCIe end-point* interface and provides *electrical power* to the Coaxlink card.

PCI Express end-point type per product

Product	Type
1629 Coaxlink Duo PCIe/104-EMB	"4-lane Rev 2.0 PCIe end-point" below
1634 Coaxlink Duo PCIe/104-MIL	"4-lane Rev 2.0 PCIe end-point" below

4-lane Rev 2.0 PCIe end-point

Applies to: Duo104EMB Duo104MIL

The 4-lane Rev 2.0 PCIe end-point:

- complies with Revision 2.0 of the PCI Express Card Electromechanical specification.
- supports 1-lane, 2-lane, and 4-lane link width
- supports PCIe Rev 2.0 link speed (5.0 GT/s with 8b/10b coding)
- supports PCIe Rev 1.0 link speed (2.5 GT/s with 8b/10b coding)
- supports payload size up to 512 bytes
- offers the optimal performance when it is configured for 4-lane PCIe Rev 2.0 link speed (5 GT/s)

4-lane Rev 3.0 PCIe end-point to PC memory data transfer performance

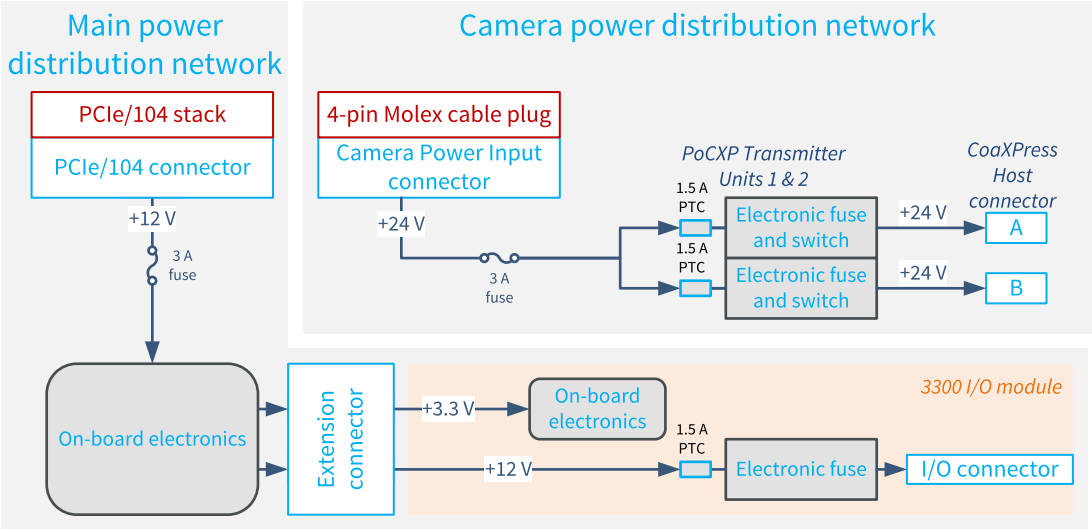
Parameter	Conditions	Min.	Typ.	Max.	Unit
Sustainable output data rate	4-lane @ 5 GT/s (PCIe Rev 2.0)		1,600		MB/s
	4-lane @ 2.5 GT/s (PCIe Rev 1.0)		800		MB/s
	2-lane @ 5 GT/s (PCIe Rev 2.0)		800		MB/s

3.3. Power Distribution Schemes

1629 Coaxlink Duo PCIe/104-EMB Power Distribution Scheme

The power distribution scheme has two distinct distribution networks:

- The main power distribution network
- The camera power distribution network



NOTE
The fuses are not serviceable! When blown, the card must be returned to the factory.

NOTE
PTCs and electronic fuses are self-resettable fuses.

NOTE
The Coaxlink card can be operated without applying power to the camera power distribution network.

The *main power distribution network* delivers power to *all the on-board electronic devices* including FPGA, memory chips, CoaXPress transceivers, I/O drivers and receivers, fan motor.

It also delivers +3.3 V and +12 V to the **3300 HD26F I/O module for Coaxlink Duo PCIe/104** plugged on the extension connector:

- The +3.3 V is used for powering the on-board electronics: I/O drivers, I/O receivers
- The +12 V is used for delivering power on the I/O connector. A PTC inserted at the input prevents potential fire hazards.

The network is fed by the Host PC through the +12 V power rail of the PCIe/104 connector. A protection fuse prevents potential fire hazards. The *+12 V LED* indicates the presence of +12 V after the protection fuse.

The *board status LED* reflects the global status of all the power converters of the main distribution network.

The *auxiliary power distribution network* delivers power to the CoaXPress cameras using the PoCXP capability available on all connections of the CoaXPress Host connector.

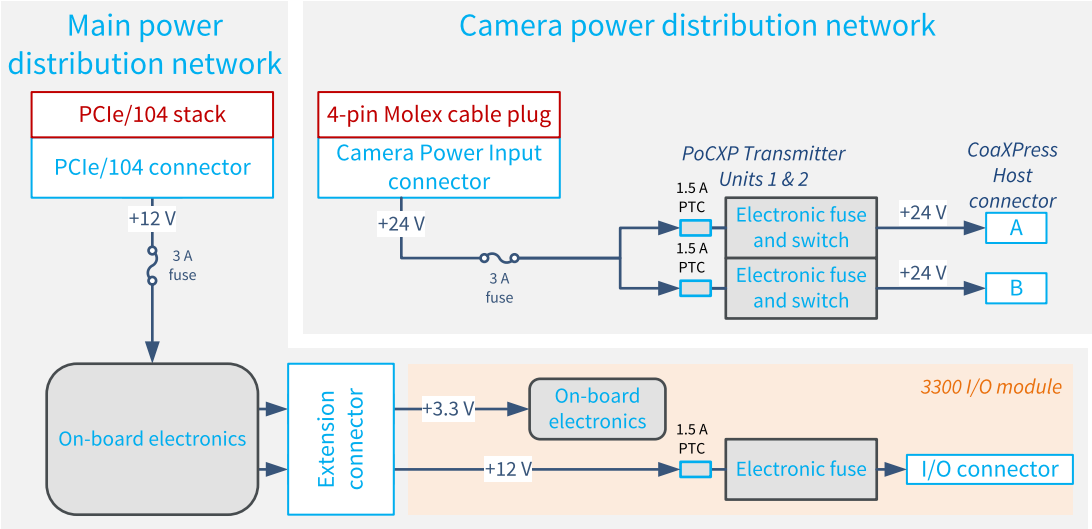
The network is fed by a 24 VDC external power supply attached to the *camera power input connector* using a power cable terminated by a 4-pin Molex plug connector. A protection fuse inserted at the input side prevents potential fire hazards.

The 24-volt DC power is applied to each camera connection through a PoCXP transmitter unit. Each PoCXP transmitter unit implements an electronic fuse/switch. A PTC inserted at the input of each transmitter unit prevents potential fire hazards.

1634 Coaxlink Duo PCIe/104-MIL Power Distribution Scheme

The power distribution scheme has two distinct distribution networks:

- The main power distribution network
- The camera power distribution network



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NOTE
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The *main power distribution network* delivers power to *all the on-board electronic devices* including FPGA, memory chips, CoaXPress transceivers, I/O drivers and receivers, fan motor.

It also delivers +3.3 V and +12 V to the I/O module plugged on the extension connector:

- The +3.3 V is used for powering the on-board electronics: I/O drivers, I/O receivers
- The +12 V is used for delivering power on the I/O connector. A PTC inserted at the input prevents potential fire hazards.

The network is fed by the Host PC through the +12 V power rail of the PCIe/104 connector. A protection fuse prevents potential fire hazards. The *+12 V LED* indicates the presence of +12 V after the protection fuse.

The *board status LED* reflects the global status of all the power converters of the main distribution network.

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The network is fed by a 24 VDC external power supply attached to the *camera power input connector* using a power cable terminated by a 4-pin Molex plug connector. A protection fuse inserted at the input side prevents potential fire hazards.

The 24-volt DC power is applied to each camera connection through a PoCXP transmitter unit. Each PoCXP transmitter unit implements an electronic fuse/switch. A PTC inserted at the input of each transmitter unit prevents potential fire hazards.

3.4. PCI Express Power

Power requirements per product

The following table provides the typical PCI Express power consumption for each product when it operates under the following conditions:

- Acquiring image data using all CoaXPress Host Interface connections operating at their maximum speed
- Delivering image data on the PCI Express configured for the largest link width and the highest link speed
- Operating @25°C [77 °F] ambient temperature and nominal supply voltages

Product	+12 V	+3.3 V	Total	Units
1629 Coaxlink Duo PCIe/104-EMB	8.4	0	8.4	W
1634 Coaxlink Duo PCIe/104-MIL	8.4	0	8.4	W

Voltage requirements

Parameter	Min.	Typ.	Max.	Units
+3.3 V voltage	3.0	3.3	3.6	V
+12 V voltage	11.0	12.0	13.0	V

3.5. Camera Power Input

Applies to:
Duo104EMB Duo104MIL

Parameter	Conditions	Min.	Typ.	Max.	Units
DC input voltage		23	24	25	V
DC input power	1-connection PoCXP			17	W
	2-connection PoCXP			34	W

3.6. I/O Power Output

Specification of the +12 V power output of the I/O connector

A non-isolated +12 V power output is available on every I/O connector.

The power originates from an external 12 V power supply plugged into the Auxiliary Power Input connector. It is distributed from a common electronic fuse to all the I/O connectors.

The electronic fuse provides the following protections:

- Limits the inrush current during power on sequence
- Protects the Coaxlink card and the power source against overload
- Protects the Coaxlink card the power source against short-circuits.

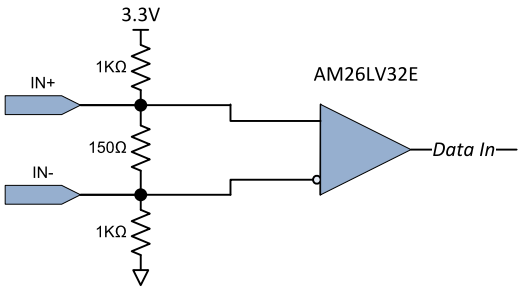
The sum of the load currents drawn from all the 12 V outputs of the I/O connectors must be lower or equal to the specified maximum output current.

I/O +12 V power output specification

Parameter	Conditions	Min.	Typ.	Max.	Units
Aggregated output current	Operating temperature range			1.0	A
Voltage drop across the electronic fuse	Max. output current			0.2	V

NOTE
The above specification applies over the whole operating temperature range of the Coaxlink card.

3.7. Differential Input



Differential Input Simplified Schematic

The receiver complies with the ANSI/TIA/EIA-422B specification.

DC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Common mode voltage		-7		+7	V
Differential sensitivity				200	mV
Input impedance			120		Ohm
ESD protection	Human Body Model (HBM)	15			kV
	Contact discharge	8			kV
	Air gap discharge	15			kV

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	100			ns
Pulse rate	0		5	MHz
10%-90% rise/fall time			1	µs

Logical map

The state of the port is reported as follows:

Relative V+/V- voltage	Logical State
V+ > V-	HIGH
V+ < V-	LOW
Unconnected input	HIGH

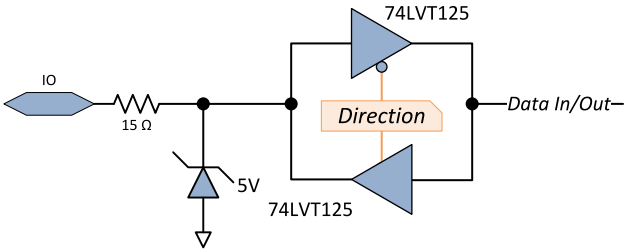
Compatible drivers

The following drivers are compatible with the high-speed differential input ports:

- RS-422/RS-485 differential line drivers
- Complementary TTL drivers

3.8. TTL Input/Output (Version 1)

Applies to:



TTL Input/Output Simplified schematic

The port implements a 3.3 V LVTTL driver and a 5 V-compliant 3.3 V LVTTL receiver.

DC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
ESD protection	Human Body Model (HBM)	2			kV

NOTE
The I/O port includes a latch-up protection.

Driver

Parameter	Conditions	Min.	Typ.	Max.	Units
Low-level output current				64	mA
Low-level output voltage	@ 8 mA		0.34	0.36	V
	@ 16 mA		0.48	0.55	V
	@ 32 mA		0.78	0.81	V
	@ 64 mA		1.34	1.36	V
High-level output current				-32	mA
High-level output voltage	@-8 mA; (1)	2.60	3.00		V
	@-16 mA; (1)	2.20	2.70		V
	@-32 mA; (1)	1.75	2.20		V
ESD protection	Human Body Model (HBM)	2			kV

Condition (1): 300 Ohms line termination resistor to GND.

Receiver

Parameter	Conditions	Min.	Typ.	Max.	Units
Absolute maximum voltage rating		0		5	V

AC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Pulse width		100			ns
Pulse rate		0		5	MHz
10%-90% rise/fall time	(1)		10	20	ns

Condition (1): Short cable (1 m) and a 300 Ohms line termination resistor to GND.

Logical Map

The state of the port is reported as follows:

Input voltage	Logical State
VIN > 2.0 V	HIGH
VIN < 0.8 V	LOW
Unconnected input port	*Undetermined*

Compatible sources

Sources with the following drivers are compatible:

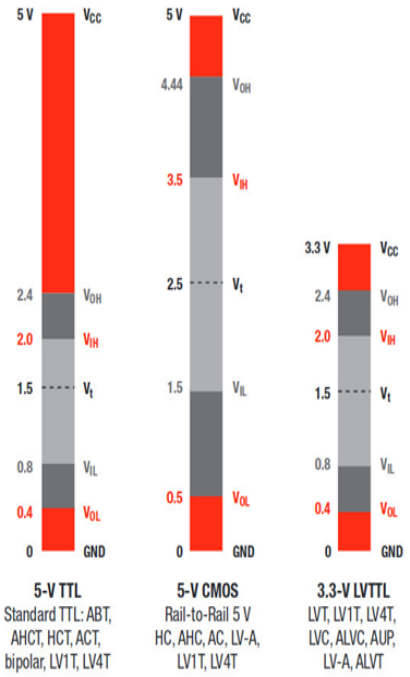
- LVTTL (3.3 V low-voltage TTL)
- TTL (5 V TTL)
- CMOS (5 V CMOS)

Compatible loads

Loads with the following receivers are compatible:

- LVTTL (3.3 V low-voltage TTL)
- TTL (5 V TTL)

3.9. TTL, 5 V CMOS and LVTTL Levels



Colors legend

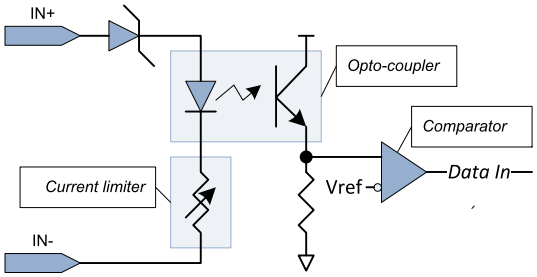
- Dark gray: noise margin,
- Light gray: transition range, low and high level are unspecified

Voltage levels

- $V_{IL:}$ maximum low-state voltage @receiver input
- VIH: minimum high-state voltage @receiver input
- $V_{OL:}$ maximum low-state voltage @driver output
- $V_{OH:}$ minimum high-state voltage @driver output
- V_t: threshold level, typically at the middle of the transition range

3.10. Isolated Input

Specification of the isolated GPIO input ports

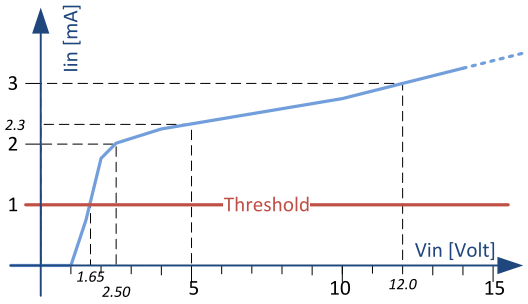


Isolated Input Simplified schematic

The input port implements an isolated current-sense input.

DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Differential voltage		-30		+30	V
Input current threshold			1		mA
Differential voltage	@1 mA	1.5	1.65	1.9	V
Input current	@(VIN+ - VIN-) = 1.65 V		1		mA
	@(VIN+ - VIN-) = 2.5 V		2		mA
	@(VIN+ - VIN-) = 5 V		2.3		mA
	@(VIN+ - VIN-) = 12 V		3		mA
	@(VIN+ - VIN-) = 30 V			5	mA
	@(VIN+ - VIN-) < 1 V			10	µA
DC isolation voltage		250			V
AC isolation voltage		170			V_{RMS}



Input Current vs. Input Voltage Characteristics

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse width	10			µs
Pulse rate	0		50	kHz

Logical map

The state of the port is reported as follows:

Input current	Logical State
IIN > 1 mA	HIGH
IIN < 1 mA	LOW
Unconnected input port	LOW

Compatible drivers and receivers

The following drivers are compatible with the isolated current-sense inputs:

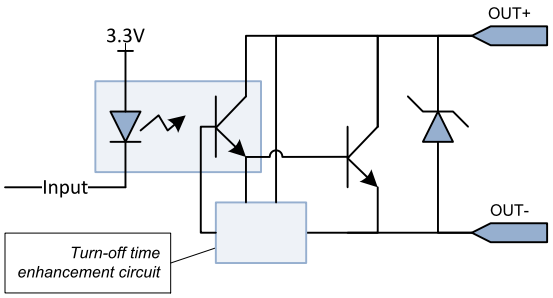
- Totem-pole LVTTL, TTL, 5 V CMOS drivers
- RS-422 Differential line drivers
- Potential free contact, solid-state relay, or opto-isolators
- 12 V and 24 V signaling voltages are also accepted

NOTE

- The +12 V power supply on the I/O connector(s) can be used for powering drivers requiring a power supply.
- No external resistors are required. However, to obtain the best noise immunity with 12 V and 24 V signaling, it is recommended to insert a series resistor in the circuit. The recommended resistor values are: 4.7k Ohms for 12 V signaling and 10k Ohms for 24 V signaling.

3.11. Isolated Output

Specification of the isolated GPIO output ports



Isolated Output Simplified schematic

The output port implements an isolated contact output.

DC characteristics>

Parameter	Conditions	Min.	Typ.	Max.	Units
Current				100	mA
Differential voltage	Open state	-30		30	V
	Closed state @ 1 mA			0.4	V
	Closed state @ 100 mA			1.0	V
DC isolation voltage		250			V
AC isolation voltage		170			V_{RMS}

NOTE

- The output port in the closed state has no current limiter, the user circuit must be designed to avoid excessive currents that could destroy the output port.
- The output port remains in the OFF-state until it is under control of the application.

AC characteristics

Parameter	Min.	Typ.	Max.	Units
Pulse rate	0		100	kHz
Turn-on time			5	µs
Turn-off time			5	µs

Typical switching performance @ 25°C

Current [mA]	Turn ON time [µs]	Turn OFF time [µs]
0.5	2.0	4.8
1.0	2.0	3.9
4.0	2.2	3.3
10	2.3	2.7
40	2.3	2.7
100	2.3	2.7

Logical map

The state of the output port is determined as follows:

Logical State	Output port state
HIGH	The contact switch is closed (ON)
LOW	The contact switch is open (OFF)

Compatible loads

The following loads are compatible with the isolated contact output ports:

- Any load within the 30 V / 100 mA envelope is accepted. The power originates from an external power source or alternatively from the power delivered through the 12 V and GND pins of the I/O connectors.

4. Environmental Specification

Environmental specification of the product(s) including: climatic requirements, electromagnetic standards compliance statements, safety standards compliance statements, etc.

4.1. Environmental Conditions

Storage and operating conditions specification of standard climatic class products

Storage Conditions

Applies to:
Duo104EMB 3300 3301 3302

Parameter	Conditions	Min	Max	Units
Ambient air temperature		-20 [-4]	70 [158]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

Applies to:
Duo104MIL

Parameter	Conditions	Min	Max	Units
Ambient air temperature		TBD	70 [158]	°C [°F]
Ambient air humidity	Non-condensing	TBD	TBD	% RH

Operating Conditions

Applies to:
Duo104EMB 3300 3301 3302

Parameter	Conditions	Min	Max	Units
FPGA die temperature			80 [176]	°C [°F]
Ambient air temperature		0 [32]	55 [131]	°C [°F]
Ambient air humidity	Non-condensing	10	90	% RH

Applies to:
Duo104MIL

Parameter	Conditions	Min	Max	Units
FPGA die temperature			100 [212]	°C [°F]
Ambient air temperature	Conduction-cooling	-40 [-40]	85 [185]	°C [°F]
Ambient air humidity	Non-condensing	0	100	% RH
Shock amplitude	All axes – 11 ms duration – Half-sine and saw tooth pulse shapes		20	g

WARNING
The thermal design of the host PC must ensure that, at any time, the FPGA die temperature never exceeds the recommended limit.

WARNING
Exceeding the upper limit of the FPGA die temperature can permanently damage the card.

NOTE
For PCIe/104 products only, the ambient air temperature specification applies to any point in the vicinity of the module including the gap between modules of the PCIe/104 stack.

4.2. Temperature Monitor

FPGA die temperature sensor

All Coaxlink frame grabbers embed a temperature sensor on the FPGA die.

When the TemperatureSensorSelector feature of the Interface Module is set to Grabber, the Temperature feature of the Interface Module reports the FPGA die temperature expressed in °C.

The user application is invited to check regularly the FPGA die temperature to ensure that the board operates within the specified operating limits.

See also: "Environmental Conditions" on the previous page

FPGA die temperature warning

Applies to:

When the measured FPGA die temperature reaches *87°C*, these Coaxlink products post a *"FPGA temperature is too high"* Memento message.

The *"FPGA temperature is too high"* message is sent repeatedly every second until the measured temperature decreases below 83°C or increases above 103°C.

TIP
Operation is still possible but is not recommended!

WARNING
When such event occurs, the user is invited to check and, possibly, improve the card cooling in the host PC!

FPGA die temperature error

Applies to:

Random errors could occur in the FPGA if its core temperature becomes excessive. Therefore, for security reasons, the stream acquisition is stopped when the measured FPGA die temperature reaches 103°C!

The *"FPGA temperature is too high; stopping operation to prevent damaging the card"* Memento message is sent repeatedly every second until the measured temperature decreases below 97°C.

TIP
Stopping the acquisition reduces significantly the heat production of the FPGA. This action is aimed to reduce the die temperature, to prevent the application against unexpected FPGA behavior and to prevent damaging the card.

WARNING
When such event occurs, the user must immediately shut down the system and revise the card cooling in the host PC before restarting!

4.3. Thermal Data

The main heat contributors are:

1. The electronic devices of the Coaxlink card including the losses of the power converters of the *main* power distribution network.
2. The losses of the 12V-24 V power converter of the *auxiliary* power distribution network of Coaxlink PCIe products. The actual contribution depends on the effectively delivered PoCXP power!

> **NOTE**
> The losses of the 12V-24 V power converter are estimated with 17 W* of PoCXP output power per connector and a worst case 24 V DC/DC converter efficiency of 92.5%.
> (*) 25 W for **3621-LH Coaxlink Mono CXP-12 LH**

Generated heat power estimation and cooling method

The following table shows the estimated heat power generated by the card for two use cases:

1. *Heat power 1:* when the card doesn't deliver any PoCXP power
2. *Heat power 2:* when the card delivers the maximum PoCXP power on all connectors.

Product	Heat power 1	Heat power 2	Cooling method
1629 Coaxlink Duo PCIe/104-EMB	8.4 W	8.4 W	Conduction
1634 Coaxlink Duo PCIe/104-MIL	8.4 W	8.4 W	Conduction

Requirements for conduction-cooled products

The heat produced by the board is conducted to the chassis enclosure using a heatsink such as the **3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104**

The thermal design of the PCIe/104 system must ensure an adequate cooling of the enclosure to keep the FPGA die temperature and the ambient air temperature below the upper limits of the allowed temperature range. The application is responsible for regularly checking the temperature and for taking the appropriate action in case of excessive temperature.

4.4. Compliances

Compliance statements.

CE compliance statement

Applies to:

Duo104EMB | 3300 | 3301 | 3302

Notice for Europe

This product is in conformity with the Council Directive 2014/30/EU

This piece of equipment has been tested and found to comply with Class B EN55022/CISPR22 electromagnetic emission requirements and Class A EN55024/CISPR24 electromagnetic susceptibility.

This product has been tested in typical class A and class B compliant host systems. It is assumed that this product will also achieve compliance in any class A or class B compliant unit.

To meet EC requirements, shielded cables must be used to connect a peripheral to the card.

CE compliance statement

Applies to:

Duo104MIL

Notice for Europe

This product is in conformity with the Council Directive 2014/30/EU

This piece of equipment has been tested and found to comply with Class B EN55022/CISPR22 electromagnetic emission requirements and Class A EN55024/CISPR24 electromagnetic susceptibility.

This product has been tested in typical class A and class B compliant host systems. It is assumed that this product will also achieve compliance in any class A or class B compliant unit.

To meet EC requirements, shielded cables must be used to connect a peripheral to the card.

FCC compliance statement

Applies to:

Duo104EMB | 3300 | 3301 | 3302

Notice for USA

Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation or when the equipment is operated in a commercial environment.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC compliance statement

Applies to:
Duo104MIL

Notice for USA

Compliance Information Statement (Declaration of Conformity Procedure) DoC FCC Part 15

This equipment has been tested and found to comply with the limits for Class A and Class B digital devices, pursuant to Part 15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation or when the equipment is operated in a commercial environment.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Shock and vibrations

Applies to:
Duo104MIL

Half-sine and terminal peak shocks according to MIL-STD-810G method 516.6:

- 40 g/11 ms

RoHS compliance statement

This product is in conformity with the European Union 2015/863 (ROHS3) directive, that stands for "the restriction of the use of certain hazardous substances in electrical and electronic equipment".

REACH statement

This product is in conformity with the European Union 1907/2006 (REACH) regulation.

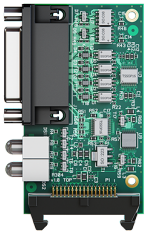
WEEE statement

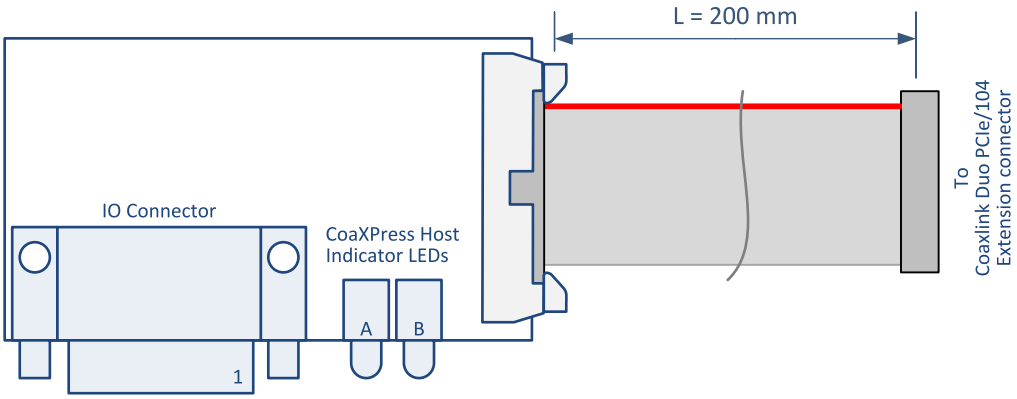
According the European Union 2012/19/EU directive, the product must be disposed of separately from normal household waste. It must be recycled according to the local regulations.

5. Related Products & Accessories

5.1. 3300/3302 Accessories for Coaxlink Duo PCIe/104

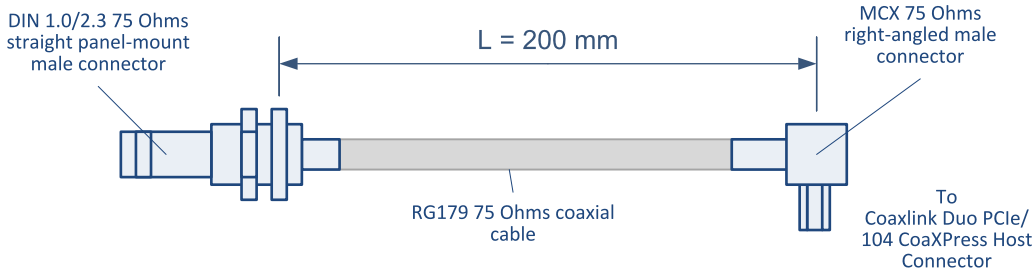
3300 HD26F I/O module for Coaxlink Duo PCIe/104





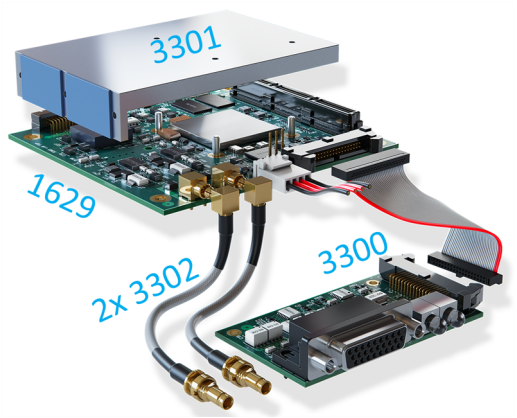
- "3300 I/O Connector" on page 14
- "CoaXPress LED lamps" on page 19

3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104



- "3302 DIN 2 CoaXPress Host Connector" on page 11

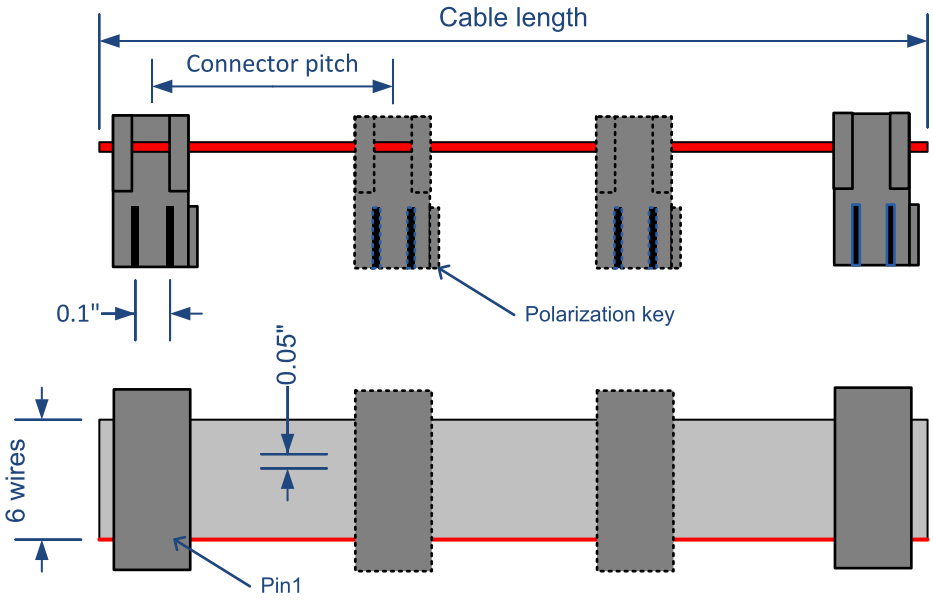
Coaxlink Duo PCIe/104 assembly



1629 Coaxlink Duo PCIe/104-EMB with 3300 HD26F I/O module for Coaxlink Duo PCIe/104 , 3301 Thermal drain (Model 1) for Coaxlink Duo PCIe/104 and 2 3302 DIN1.0/2.3 Coaxial cable for Coaxlink Duo PCIe/104

5.2. Custom C2C-Link Ribbon Cable Assembly

Assembly instructions of a custom-made IntraPC C2C-Link interconnection.



Custom C2C-Link Ribbon Cable Assembly

The cable assembly is composed with:

- A piece of a 6-conductor 0.05-in pitch ribbon cable. For instance: *Belden's (9L280XX Series)*.
- Two or more pieces of a 2 x 3-pin female ribbon cable connectors. For instance: *TE connectivity 1-1658528-1*.

The cable assembly has:

- A maximum of 4 connectors allowing up to 4 cards to share the same C2C-Link.
- A maximum length of 60 cm.

NOTE
The connector pitch(es) must be determined according to the actual card to card spacing in the Host PC.